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9100 UMOD

Universal Modem 1–PAK Chassis

Installation and Operation Manual

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Chapter 1
Introduction

The Hughes Network Systems, Inc. (HNS) 9100 Universal Modem (UMOD) is a high-performance multifunction satellite modem providing features that include multiple bit rates, modulation types, coding schemes, terrestrial interfaces, and IF frequency bands. The UMOD is operational as:

- A standalone, open–network modem for use with INTELSAT (IDR/IBS) and EUTELSAT (SMS) standards.
- A standalone modem for closed networks.
- An integral part of the HNS Gemini VSAT, a private digital data network for economical bypass of terrestrial data lines.

The 9100 UMOD is available in a single modem chassis referred to as the 1–PAK as shown in figure 1-1 and in a ten–modem chassis called the 10–PAK. The 10–PAK is described in the *9100 UMOD Universal Modem 10–PAK Chassis Installation and Operation Manual*, HNS document number 8051364.

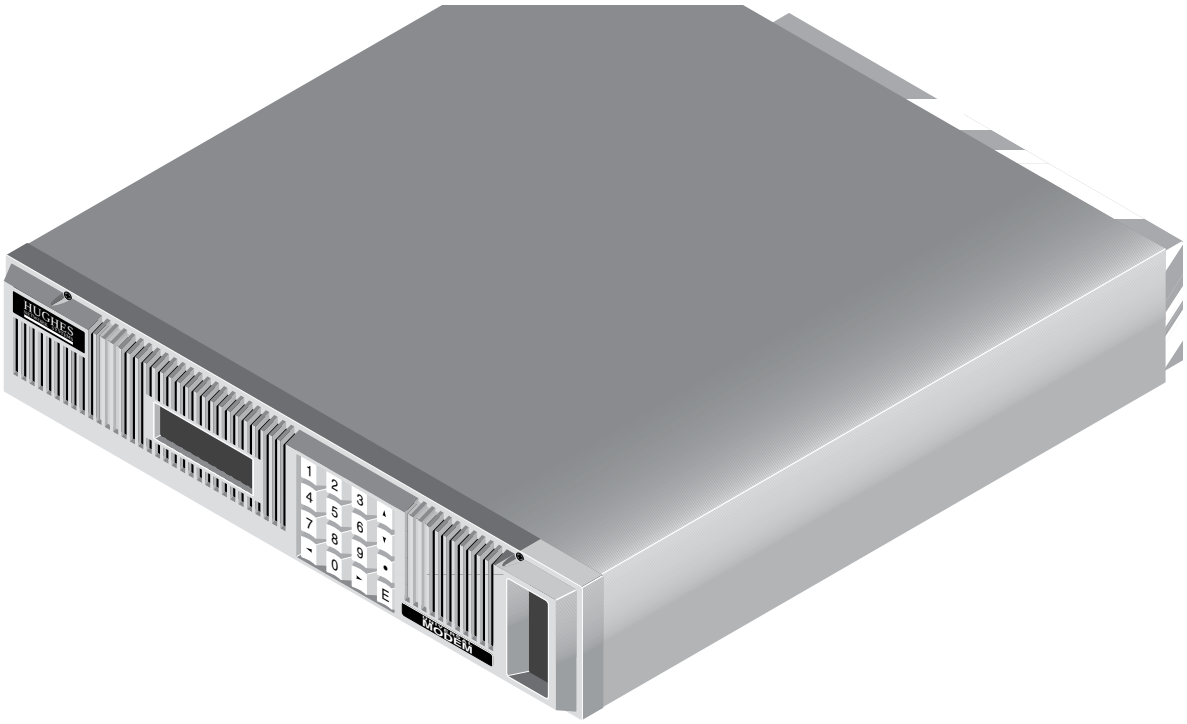

Figure 1-1 The 9100 Universal Modem single-modem chassis (1-PAK)

The UMOD supports IDR/IBS/SMS framing, single- or twin-bearer drop-and-insert (D&I) multiplexing, an internal bit

error rate test set, and an E_bN_o monitor for use in Single Channel Per Carrier (SCPC) and Multiple Channel Per Carrier (MCPC) systems. Figure 1-2 shows a typical SCPC/MCPC application.

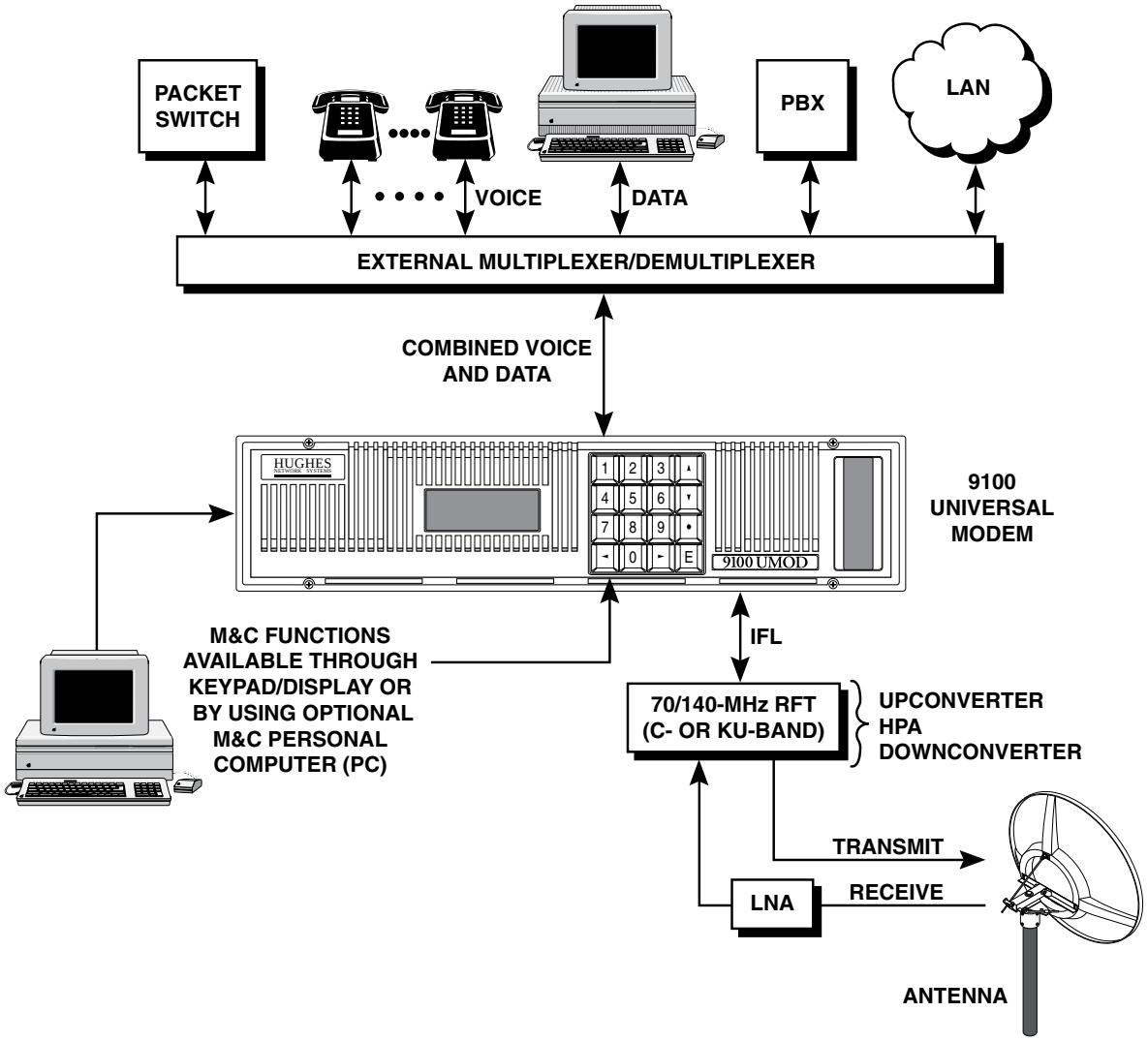

Figure 1-2 Typical SCPC/MCPC application

The UMOD meets the requirements demanded of modern satellite modems as well as several features that offer flexibility for growth from simple SCPC point-to-point applications to fully-networked point-to-multipoint operation:

- Universal feature set—The feature set covers both current and future applications with multiple bit rates, software selectable in 1-bps increments from 9.6 kbps to 8.448 Mbps; BPSK and QPSK modulation methods; Viterbi,

Sequential, Reed-Solomon, and Concatenated FEC coding; Internal framing to support IDR, IBS, and SMS framing, single- and twin-bearer D&I multiplexing, and Engineering Service Channel (ESC) supervisory overhead. All features are software-selectable, *there are no switches or jumpers to configure*.

- Single-card design—The entire modem, framing unit, and multiple terrestrial and IF interfaces are integrated into a single circuit board.
- Application-Specific Integrated Circuits (ASICs)—The single-card design is made possible by using several HNS-developed ASICs to perform UMOD functions.
- Bit rate: 9.6 kbps to 8.448 Mbps (selectable in 1-bps increments)
- Baseband interface: RS-232, RS-422/449, V.35, or G.703 (T1, E1, T2, and E2)
- IF/RF interface: 70 MHz, 140 MHz, or L-Band
- Modulation methods: BPSK and QPSK
- FEC coding compatibility: Viterbi, Sequential, Concatenated Viterbi/Reed-Solomon
- Internal framing unit supports IDR, IBS, and SMS framing, single- and twin-bearer D&I multiplexing, and ESC supervisory overhead
- Full redundancy switchover option in 1-for-1 (1:1) redundancy

Chapter 2

Specifications

This chapter lists UMOD physical, enironmental, system, modulator, and demodulator specifications.

2.1

Physical dimensions

This section provides physical specifications for the Universal Modem 1-PAK chassis.

1-PAK chassis

Weight: 22.5 pounds (10.2 kg)

Refer to figure 2-1 for height, width, and depth dimensions.

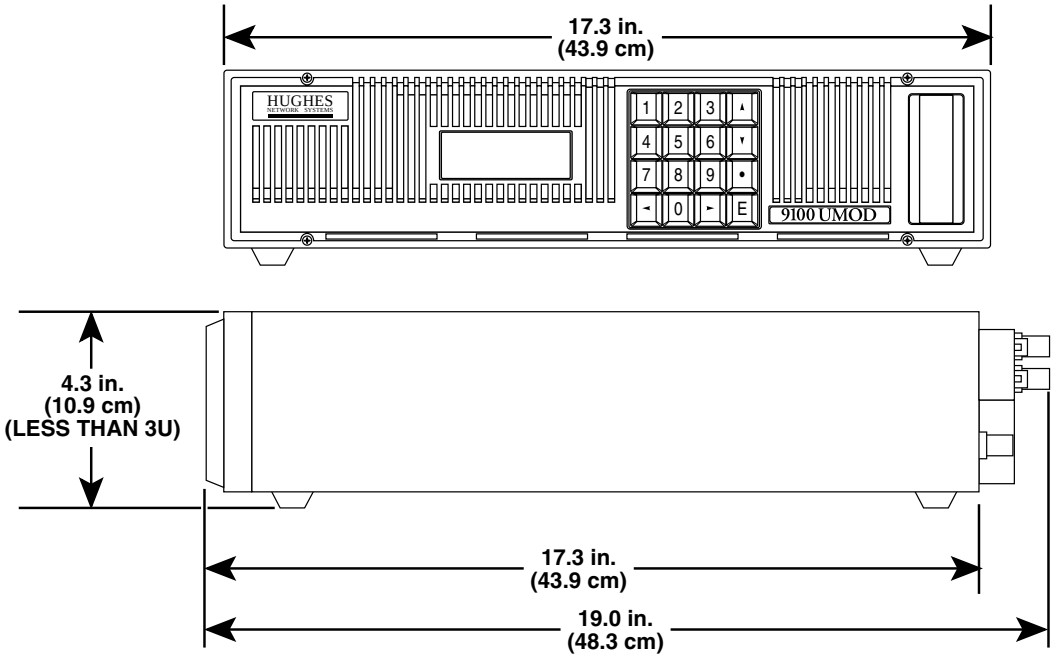

Figure 2-1 1-PAK chassis physical dimensions

2.2

Environmental specifications

This section describes the 9100 UMOD single-modem chassis temperature, altitude, and humidity specifications.

Temperature

The temperature requirements are:

- Operating range: 32 °F to 122 °F (0 °C to 50 °C)
- Storage range: -40 °F to 167 °F (-40 °C to 75 °C)

Altitude

The altitude requirements are:

- Maximum operating altitude: 15,000 feet (4,752 meters)
- Maximum non-operating altitude: 50,000 feet (15,240 meters)

Humidity

The humidity requirements are:

- Maximum operating humidity: 95% relative humidity (RH) at 122 °F (50 °C)
- Minimum operating humidity: 5% RH at 122 °F (50 °C)

2.3

System specifications

This section describes 9100 Universal Modem system specifications.

Single slot chassis power consumption

Single slot chassis (117VAC, 60 Hz) power consumption, see table 2-1 .

Table 2-1 Power Usage

Conditions	Typical Pwr	New Spec Pwr
PS only no Bd	61 W	
With UMOD and no RFM	122 W	150W
GEMINI with 5–watt radio	197 W	240 W

Operating frequency

Ranges: 52—88 MHz or 104—176 MHz (or 52—88 MHz *and* 104—176 MHz available as an option)

Step size: 100 Hz

Channel spacing

Less than 0.5 dB degradation with two adjacent carriers 10 dB higher at 1.4 X symbol rate

Modulation types

BPSK and QPSK

Data rates

Range: 9.6 kbps—8.448 Mbps (BPSK 9.6 Kbps – 2.048 Mbps)

Step size: 1-bps steps

Symbol rates

9.6 Ksps to 10 Msps

Forward error correction

Types: Viterbi, Sequential, Concatenated Viterbi/Reed-Solomon

Rates: 1/2, 3/4, 7/8, 1 (No coding)
(Sequential coding limited to R1/2 and 2.048 Mbps)

Data interfaces

DIM: RS-232, RS-449, V.35

GIM: G.703 (T1, balanced and unbalanced E1, balanced and unbalanced T2, E2)

Scrambling

CCITT V.35 and IESS-309 (IBS)

Reference stability

±2 ppm; ±1 ppm per year

Elastic buffer

Up to 512 Kbits or 32 ms (selectable in bytes or ms)

Configuration

Front panel, ASCII terminal, remote (Hayes command set)

Monitor and control (M&C)

Configuration, loopbacks, alarms (local or remote)

Open-network framing

Intelsat IDR and IBS (IESS-308 and IESS-309),
Eutelsat SMS (BS 7-40), or none

Engineering service channel (ESC)

IDR, IBS, or none (for Open Network Applications)

Overhead Channel

See appendix H (for Closed Network Applications)

Diagnostics

Bit Error Rate Test Function: 511-bit PN sequence; user-defined 8-bit repetitive mark/space; 1010 repetitive

Operational E_b/N_o Monitor: ±1 dB accuracy

Bit error rate performance

Uncoded: BPSK: 0.5 dB from theoretical; QPSK: 0.75 dB from theoretical in IF-Back-to-Back, (see table 2-2 on page 2–5).

Coded: Intelsat specifications are guaranteed. Table 2-2 illustrates typical performance

Redundancy switchover

Optional redundancy switchover support for all chassis is available in the following configuration:1-PAK chassis: 1-for-1

Station clock input

1 MHz to10 MHz (± 10 ppm, 100–Hz steps)

Input voltages

The 9100 Universal Modem power supply automatically adjusts to accept the following input voltage range: 1-PAK chassis: 100 to 240 Vac (47 to 63 Hz)

2.4

Modulator specifications

This section describes 9100 Universal Modem modulator specifications.

Transmit power

Transmit power: -5 dBm to -30 dBm

Resolution: 0.1 dB

Accuracy: ±0.25 dB

On/Off isolation: > 60 dB

Output impedance

50 Ω (75 Ω optional)

Output return loss

20 dB

Output frequency stability

±2 ppm all causes; ±1 ppm per year

Spectral shape

Programmable (IDR, IBS, Custom)

Spurious and Harmonics

> -50 dBc

Transmitted noise

-100 dBm/Hz at 0 dBm output level

-130 dBm/Hz at -30 dBm output level

2.5

Demodulator specifications

This section describes 9100 Universal Modem demodulator specifications.

Input power

Input impedance: 50 Ω (75 Ω optional)

Input return loss: 20 dB

Desired carrier range: -30 to -55 dBm

Aggregate: -5 dBm Composite

Acquisition range

Carrier: ±30 KHz

Clock: ±100 ppm

Bit error rate performance

Refer to section 2.3, “System specifications” and table 2-2 .

Table 2-2 9100 Universal Modem typical bit error rate vs. E_b/N_o performance specifications

Modulation type	Forward Error Correction (FEC) Type	FEC Rate	E_b/N_o for BER shown below						Remarks
			1E–3	1E–4	1E–5	1E–6	1E–7	1E–10	
BPSK	None	1	8.6	9.9	10.9	11.7	12.4	–	0.5 dB from theoretical
BPSK	Convolutional/ Viterbi	1/2	3.9	4.6	5.3	5.9	6.4	–	K=7
BPSK	Convolutional/ Viterbi	3/4	5.1	5.7	6.2	6.8	7.3	–	K=7
BPSK	Convolutional/ Viterbi	7/8	5.9	6.6	7.5	8.3	9.3	–	K=7
BPSK	Sequential	1/2	–	3.8	4.3	4.8	5.3	–	56Kbps
BPSK	Sequential	1/2	–	4.5	4.9	5.3	5.7	–	1Mbps
BPSK	Sequential	1/2	–	4.7	5.1	5.4	5.8	–	2Mbps
BPSK	Concatenated Vit/R–S	1/2,201 /219	–	–	–	–	–	4.3	K=7
BPSK	Concatenated Vit/R–S	3/4,201 /219	–	–	–	–	–	5.8	K=7
QPSK	None	1	8.9	10.1	11.1	11.9	12.6	–	0.75 dB from theoretical
QPSK	Convolutional/ Viterbi	1/2	4.1	4.8	5.5	6.1	6.6	–	K=7
QPSK	Convolutional/ Viterbi	3/4	5.3	5.9	6.4	7.0	7.5	–	K=7
QPSK	Convolutional/ Viterbi	7/8	5.9	6.8	7.6	8.3	9.1	–	K=7
QPSK	Sequential	1/2	–	4.0	4.5	5.0	5.5	–	56Kbps
QPSK	Sequential	1/2	–	4.7	5.1	5.5	5.9	–	1Mbps
QPSK	Sequential	1/2	–	5.0	5.3	5.7	6.0	–	2Mbps
QPSK	Concatenated Vit/R–S	1/2,201 /219	–	–	–	–	–	4.3	K=7
QPSK	Concatenated Vit/R–S	3/4,201 /219	–	–	–	–	–	5.8	K=7

All values are typical in IF back–to–back with V.35 scrambling and differential encoding/decoding.

Chapter 3

UMOD hardware theory of operation

The UMOD is a digital satellite modem that serves as a link between the user's baseband data terminal equipment (DTE) and the IF frequency interface with a radio or up/downconverter. In addition to the basic phase shift keying (BPSK and QPSK) functions, the UMOD performs data processing such as forward error correction (FEC), open-network framing, Doppler buffering, and data multiplexing.

UMOD functions are divided as follows:

- Transmit and receive functions. The UMOD is typically configured for full-duplex operation, transmitting user data toward the satellite and receiving data from the satellite. The two paths are independent for most applications.
- System functions. These include monitor and control (M&C), self-test diagnostics, timing generation, redundancy, loopbacks, and bit error rate testing (BERT).

Figure 3-1 on page 3–2 is a high-level diagram of the UMOD that shows transmit, receive, and system functions. The following sections describe UMOD functions in the order they appear in the figure.

3.1 Transmit operations

In the transmit direction (see figure 3-1 on page 3–2), the UMOD accepts user data at the customer interface module (CIM) and directs the data across the backplane to the transmit portion of the terrestrial data interface daughtercard (either a data interface module or a G.703 interface module) installed on the UMOD motherboard.

After the terrestrial data interface converts the data from the user's electrical format (RS-232, RS-449, V.35, or G.703) to the format used in the UMOD, the data is either routed to the UMOD motherboard, or—if there is an optional internal framing unit (IFU) installed on the UMOD motherboard—to the transmit portion of the IFU for processing. After IFU processing, the data is directed to the UMOD motherboard.

On the motherboard, the data is sent to the channel encoder, where operations such as scrambling, differential encoding, and FEC encoding are performed. After encoding, the data is routed to the transmit filter for digital filtering and interpolation; then passed to the modulator where the signal is PSK-modulated onto an IF carrier provided by the transmit synthesizer. This modulated carrier is amplified in the IF stage processor, then routed for

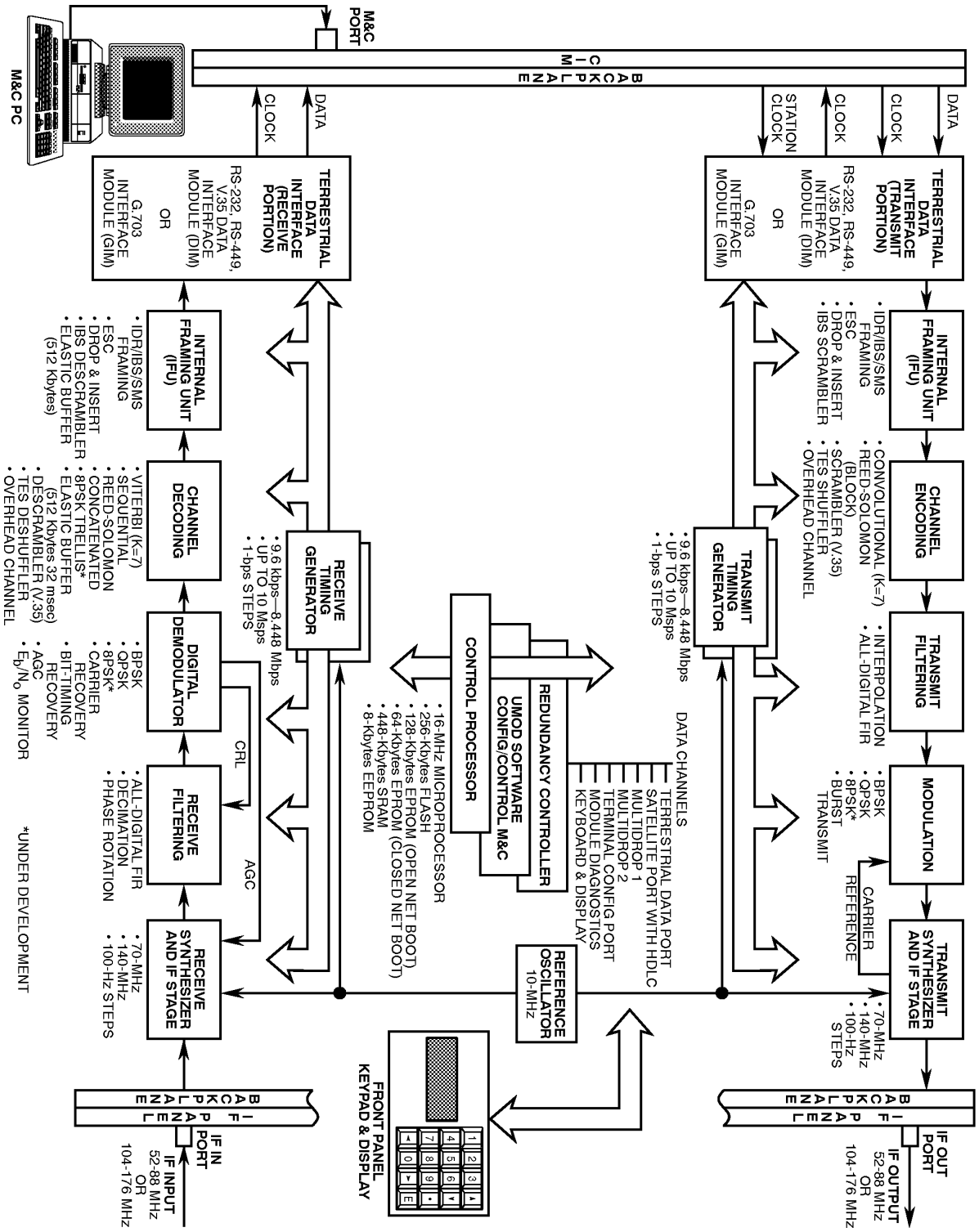

Figure 3-1 UMOD functional block diagram

transmission across the backplane to the IF OUT connector on the IF panel (located on the rear of the UMOD).

Customer interface module

The CIM is the interface between the user's equipment and the UMOD. Transmit data from the DTE device can be input to the UMOD at the CIM in the following electrical interface formats.

- EIA RS-232, EIA RS-422/449, or CCITT V.35. These formats are supported by the 37-pin connector labeled *TO DTE*.
- CCITT G.703. This format supports balanced T1 (also called DS1), balanced or unbalanced E1 (also called CEPT), balanced or unbalanced T2 (also referred to as DS2), and unbalanced E2 electrical interfaces. The balanced G.703 port is labeled *G.703 BAL*, the unbalanced G.703 ports are labeled *SD* (send data) and *RD* (receive data).

The CIM provides ports for drop-and-insert (D&I) multiplexing, and a port for Engineering Service Channel (ESC) signals for use with an optional internal framing unit (IFU). The D&I ports on the CIM are labeled *RD* (receive data), *SD* (send data), *IDI* (insert-data-in) and *DDO* (drop-data-out). ESC signals (including audio ESC, octet alignment, and backward alarms) are supported by the CIM port labeled *ESC SIGNALS*.

The CIM also has a station clock port (labeled *STATION CLK*) that can receive a 1-MHz to 10-MHz TTL or 0 dBm to +25 dBm level input.

Note

For more information about CIM ports, refer to appendix A, "CIM interface port pinout information."

Transmit traffic, D&I multiframes, ESC data, and clock signals are passed from the CIM to the backplane.

Backplane

The backplane serves as an internal electrical interface between the CIM and the UMOD motherboard. Baseband transmit data, ESC signals, D&I multiframes, and clock signals from the CIM are routed across the backplane to the UMOD motherboard.

The backplane routes the 70- or 140-MHz IF to the BNC connectors on the IF panel.

Terrestrial data interface

The terrestrial data interface daughtercard (installed on the UMOD motherboard) converts the baseband transmit data to the TTL format used by the UMOD motherboard. There are two types of data interface daughtercards:

- Data interface module (DIM)
- G.703 interface module (GIM)

DIM

The DIM provides level translation to TTL, buffering, and termination (if required) for the baseband transmit data. The DIM supports the following electrical formats: EIA RS-232 (up to 64 kbps), EIA RS-422/449 (up to 8.448 Mbps), or CCITT V.35 (up to 8.448 Mbps).

The DIM takes transmit data from the backplane, converts it to TTL level, performs retiming and phase correction on the converted data, then outputs the data and clock signals to the UMOD motherboard.

For more information on the DIM daughtercard, refer to section 3.6 on page 3–41, “Terrestrial data interface daughtercard.”

GIM

The GIM performs line decoding, jitter attenuation, level translation to TTL, and buffering, for the baseband transmit data, then outputs the resulting data to the UMOD motherboard for further processing or to the optional internal framing unit.

The GIM supports two bipolar baseband interfaces. The first (or *main*) interface is used by the UMOD for interfacing with the user DTE device and is capable of operating with mixed T1 (balanced), E1 (balanced or unbalanced), T2 (balanced or unbalanced), and E2 (unbalanced) transmit and receive data rates. The second interface, along with an optional IFU daughtercard, supports a two-bearer D&I framing multiplexer.

Transmit data entering the main G.703 interface is first converted to TTL level. The GIM then performs active jitter suppression on the signals, then codes the signal using one of the AMI/HDB3/B8ZS/B6ZS line codes. If the signal is coded for AMI, it can be scrambled using a $1 + X^3 + X^5$ scrambler, then output to the UMOD motherboard. Otherwise, the signal is output to the UMOD board—along with clock signals—once coding is complete.

Transmit frames entering the D&I interface portion of the GIM are first converted to TTL level. The GIM then performs active jitter suppression on the frames, then codes the signal using one of the AMI/HDB3/B8ZS line codes. The coded frames are then output to the internal framing unit.

For more information on the GIM daughtercard, refer to section 3.6 on page 3–41, “Terrestrial data interface daughtercard.”

Internal framing unit

The optional internal framing unit (IFU) daughtercard connects between the terrestrial data interface daughtercard (either a DIM or a GIM) and the UMOD. In open-network configurations, it provides single- or dual-bearer D&I multiplexing, and framing and buffering support for the following Intelsat and Eutelsat services:

- Intelsat Intermediate Data Rate (IDR) service
- Intelsat Business Service (IBS)
- Eutelsat Satellite Multi-Services (SMS)

IDR mode

In IDR mode, the IFU supports 64 kbps rates defined by the following services:

- 64-, 192-, and 384-kbps rates. These data rates are passed transparently without any overhead.
- 1.544-, 2.048-, 6.312-, and 8.448-Mbps rates. A 96-kbps overhead is added to the data.
- 512-kbps through 15536 kbps. For this data rate, the IFU adds an IBS-style overhead (1/15 or 6.7%). However, there is no audio ESC, and no facility for the 64-kbps revenue channel. **IBS MODE MUST BE SELECTED.**
- For IBS–style framing, use 64 kbps times *n* where *n*=1, 2, 4, 6, 8, 12, and 16.

In a standard framing operation, transmit data enters the IFU from the GIM. The IFU adds ESC supervisory information to the data, synchronously scrambles it, and then outputs the signals to the UMOD motherboard for further processing.

Except for the 1.544-, 2.048-, 6.312-, and 8.448-Mbps rates, IDR mode supports D&I operations. **FOR ALL D&I OPERATIONS, IBS MODE MUST BE SELECTED.** For a D&I operation, the T1 or E1 bearer from the DIM or GIM enters the IFU. The IFU removes (drops) preselected frames (or timeslots) from the bearer, assembles them in the framer, and (if appropriate) adds ESC supervisory information. The data is then scrambled—using the self-synchronizing scrambler specified in IESS-308 and V.35—and output to the UMOD motherboard for further processing.

IBS only mode

In IBS only mode, the IFU adds a 1/15 (or 6.7%) overhead to the data. The following services are supported:

- 48 kbps. Before satellite overhead is added, the IFU performs an X.50 conversion on the 48-kbps data. The conversion bit-stuffs the data up to 64-kbps.
- 56 kbps. The IFU performs an X.50 conversion to bit-stuff the 56-kbps data to 64-kbps.

- 64 kbps. Data rate is 68.26667 kbps (64 x 16 / 15) after overhead is added.
- 512 kbps. Data rate is 546.1333 kbps (512 x 16 / 15) after overhead is added.
- 1544 kbps. Data rate is 1647 kbps (1544 x 16 / 15) after overhead is added.

In a standard framing operation, transmit data enters the IFU from the GIM. The IFU frames the data, adds ESC supervisory information to the data, synchronously scrambles it, and then outputs the signals to the UMOD motherboard for further processing.

For a D&I operation, the T1 or E1 bearer from the GIM enters the IFU. The IFU removes (drops) preselected DS0s (or timeslots) from the bearer, assembles them in the framer, and adds ESC supervisory information. The data is then synchronously scrambled (as specified in IESS-309) and output to the UMOD motherboard for further processing.

SMS only mode

In SMS only mode, the IFU adds a 1/15 (or 6.7%) overhead to the data. A 1.152-kbps service is supported. Data rate is 1288.800 kbps (1152 x 16 / 15) after overhead is added.**IBS MODE MUST BE SELECTED.**

In a standard framing operation, transmit data enters the IFU from the DIM or GIM. The IFU frames the data, adds ESC supervisory information to the data, synchronously scrambles it, and then outputs the signals to the UMOD motherboard for further processing.

For a D&I operation, the T1 or E1 bearer from the GIM enters the IFU. The IFU removes (drops) preselected DS0s (or timeslots) from the bearer, assembles them in the framer, and adds ESC supervisory information. The data is then synchronously scrambled (as specified in IESS-309) and output to the UMOD motherboard for further processing.

IBS and SMS mode

In IBS and SMS mode, the IFU adds a 1/15 (or 6.7%) overhead to the data. The following services are supported:

- 64 kbps. Data rate is 68.26667 kbps (64 x 16 / 15) after overhead is added.
- 128 kbps. Data rate is 136.533 kbps (128 x 16 / 15) after overhead is added.
- 256 kbps. Data rate is 273.067 kbps (256 x 16 / 15) after overhead is added.

- 384 kbps. Data rate is 409.600 kbps (384 x 16 / 15) after overhead is added.
- 768 kbps. Data rate is 819.200 kbps (768 x 16 / 15) after overhead is added.
- 1536 kbps. Data rate is 1638.400 kbps (1536 x 16/15) after overhead is added.
- 1920 kbps. This is a 2048 kbps data stream with a 32-channel PCM frame format (referred to as CCITT G732 or CEPT). The 30 timeslots available to the user yield the 1.920 Mbps rate. The terrestrial rate is therefore 2048 kbps, not 1920 kbps.

  Because the G723 format already has a 32 / 30 overhead factor (actual rate / available rate) there is no satellite overhead, and some bits of TS0 are borrowed for satellite use. The IFU provides the option to leave the spare TS0 bits transparent end-to-end, or to set the bits “high” over the satellite link.
- 2048 kbps (unformatted). Data rate is 2184.533 kbps. At this rate, the 2184.533 kbps is handled as if it were unformatted, and the 16/15 overhead is added. No frame formatting is required. If the signal is a G732 signal, all bits are passed transparently.

In a standard framing operation, transmit data enters the IFU from the DIM or GIM. The IFU frames the data, adds ESC supervisory information to the data, synchronously scrambles it, and then outputs the signals to the UMOD motherboard for further processing.

For a D&I operation, the T1 or E1 bearer from the GIM enters the IFU. The IFU removes (drops) preselected frames (or timeslots) from the bearer, assembles them in the framer, and adds ESC supervisory information. The data is then synchronously scrambled (as specified in IESS-309) and output to the UMOD motherboard for further processing.

For more information on the IFU daughtercard, refer to section 3.7 on page 3–51, “Internal framing unit daughtercard.”

Overhead channel

A user–definable overhead channel is available for closed network applications. See appendix H for details.

Channel encoding

88The channel encoding section of the UMOD motherboard formats the data before it is modulated.

The encoding circuitry (see figure 3-2 on page 3–8) performs the functions specified in IESS-308 (IDR) and IESS-309 (IBS) that relate to forward error correction and scrambling. [In addition, this circuit performs the channel coding functions required to operate in a closed HNS Telephony Earth Station (TES) network as well as the HNS Personal Earth Station (PES) network.]

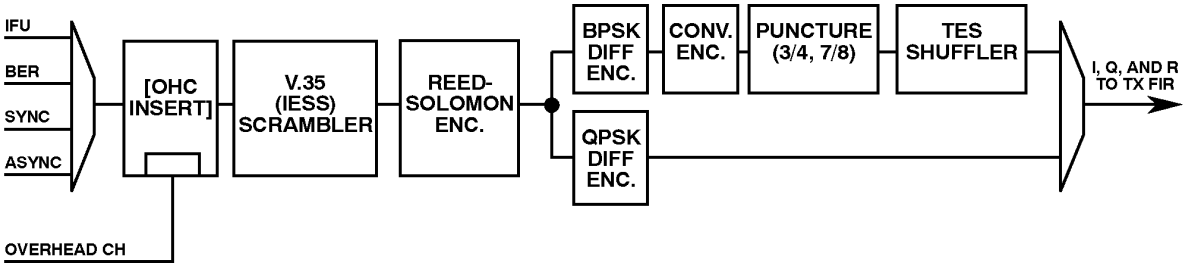

Figure 3-2 Channel encoding circuit block diagram

The channel encoding circuit performs the following functions:

- Scrambling data for energy dispersion purposes
- [Inserting the Overhead Channel Frame Marker and Data Packet]
- Differential encoding for resolution of phase ambiguity in the demodulator during initial acquisition and following cycle slips
- Converting FEC Rate 1/2 to Rate 3/4 or Rate 7/8 (Puncturing)
- FEC convolutional encoding
- Reed-Solomon encoding (IESS-308 Rev. 6A)
- 4-level interleaver per IESS-308.
- Concatenated Viterbi/Reed-Solomon encoding

The encoding circuit operates in the following modes:

- BPSK—Rate 1 (no FEC); Rates 1/2, 3/4, and 7/8 Viterbi only; Rate 1/2 Sequential only; Rates 1/2 and 3/4 with Viterbi and Reed-Solomon concatenated
- QPSK—Rate 1; Rates 1/2, 3/4, and 7/8 Viterbi only; Rate 1/2 Sequential only; Rates 1/2 and 3/4 with Viterbi and Reed-Solomon concatenated

Channel coding transmit interfaces

Text inside of brackets—[ ]—denotes features currently under development.

The channel coding circuitry interfaces to the internal framing unit or directly to the terrestrial interface via processor control. Serial data from either source is processed by the transmit channel coding and then routed to the modulator interface where preamble and postamble insertion occurs only when in TES mode of operation. During BPSK and QPSK operation transmit symbol rate data at the modulator interface consists of two serial channels: I and Q. When BPSK modulation is selected only the I channel is used.

Scrambling

Data scrambling ensures uniform spectral spreading of the transmitted carrier. Two types of scramblers are provided: IESS-309 (IBS) and V.35.

The IESS-309 (IBS) scrambler is selected when the UMOD is operating in an IBS network. To aid the descrambling synchronization process, the sequence 001001001001001 is loaded at the start of each multiframe. In addition, the frame alignment and message fields (bytes 0 and 32 respectively) of the IBS frame are left unscrambled for the same purpose. Loading of the synchronization sequence and disabling of the scrambler output during bytes 0 and 32 is controlled by the internal framing unit.

The V.35 scrambler used when operating within an IDR or TES network is self-synchronizing and meets CCITT V.35 specifications. The scrambler is reset to a known state between bursts and is enabled during a burst. When operating in TES asynchronous data (burst) mode the preamble and postamble portions of the burst are not scrambled. Only the message segment of a burst is scrambled.

Differential encoding

The channel encoding section supports both binary-phase shift keying (BPSK) and quadrature-phase shift keying (QPSK) differential encoding. When BPSK modulation is used, the BPSK differential encoder and BPSK differential decoder resolve 180-degree phase ambiguity in the received data when a demodulator carrier cycle slip causes inversion of the data. Because the Viterbi decoder will decode and correct errors but produce inverted data in such an event, biphase differential coding is required. In the case of QPSK modulation the QPSK encoder and decoder resolve 90-degree phase ambiquity.

The QPSK differential encoder is used only in R1 QPSK; the BPSK encoder is used for BPSK, and QPSK, when in Viterbi or Viterbi-Reed-Solomon modes. The selection of differential coding type is software controlled.

Forward error correction encoding

The following is a list of the forward error correction (FEC) encoding methods supported by the UMOD channel coding section:

- Rate 1/2, 3/4, and 7/8 convolutional encoding (K=7)
- Rate 1/2 and 3/4 convolutional encoding (K=36)
- Rate 1/2 and 3/4 concatenated Viterbi and Reed-Solomon encoding
- 4-level interleaver used with Reed-Solomon encoder (per IESS-308)

TES shuffler

This circuit is included as part of the UMOD channel coding to allow compatible operation within a TES network.

Modulator interface (preamble and postamble insertion)

This circuit is included as part of the UMOD channel coding to allow compatible operation within a TES network.

Transmit filtering

Transmit filtering is performed digitally on the data from the channel encoding section (see figure 3-3 on page 3–11). Dual finite impulse response (FIR) filters—part of the FIR/NCO ASIC—perform baseband spectral shaping on the I and Q channels. To meet UMOD requirements, the filter coefficients are programmable, not fixed. In most cases either a linear-phase raised-cosine filter or a square-root raised-cosine filter response is used, although the FIR filter is capable of almost any response desired, including Butterworth and Bessel responses. Corrections for sinx/x distortions in the digital-to-analog (D/A) converter are included in the filter coefficient set.

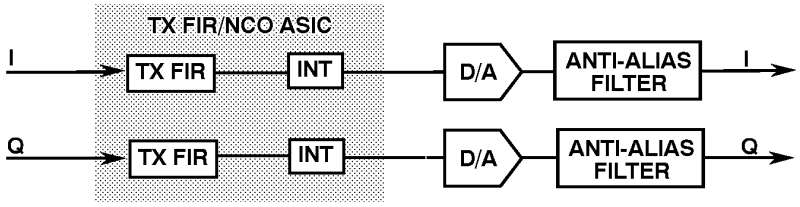

Figure 3-3 Transmit filter circuit block diagram

Alias spectra will appear at multiples of the sampling rate of the FIR filter which lie within the passband of the anti-alias filter. To remove these spectral components, a series of interpolation filters are used after the main FIR filter to upsample the data from the FIR filter to a final sample rate in the range of 10 to 20 Msps. This upsampling places the alias components within the stopband of the anti-alias filters.

Following the FIR filters, D/A converters convert the digital output sequence into rectangular pulses whose amplitude is proportional to the value of the data word.

The D/A converters are followed by fixed-bandwidth anti-alias filters to suppress the alias spectra created by the discrete time nature of the FIR filter. The cutoff frequency of the lowpass filters is approximately 5 MHz to accommodate the highest design symbol rate of 9.3 Msps. The filter incorporates group-delay equalization.

Modulator

Filtered I and Q channels are input to an analog quadrature amplitude modulator to generate the desired modulation (see figure 3-4 on page 3–12). BPSK and QPSK modulation formats are supported.

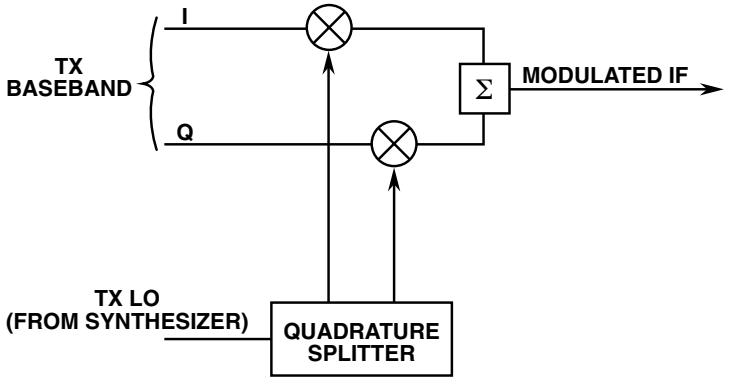

Figure 3-4 Modulator circuit block diagram

The phase of the local oscillator (LO) signal from the transmit synthesizer is split into 0- and 90-degree quadrature signals by an integral phase splitter in the modulator. The LO frequency is at the desired carrier frequency, so that the conversion from baseband to IF takes place in a single step. This approach avoids the spurious output signals caused by more complicated multiple conversion transmit IF chains.

Transmit synthesizer

The transmit synthesizer generates the LO at the desired carrier frequency (see figure 3-5 on page 3–13). The requirements of a wide LO tuning range (52 to 88 MHz and 104 to 176 MHz) and a small step size (less than 100 Hz) result in a cascaded-synthesizer design. The first synthesizer in the chain is a numerically-controlled oscillator (NCO) that is part of the FIR/NCO application-specific integrated circuit (ASIC). The NCO is constructed from a phase accumulator that generates a digital phase ramp whose phase increment is programmable. The ramp is converted to a digital sinusoid by a sine wave lookup table. The output of the lookup table is quantized to the required number of bits, and is processed by a noise-shaping filter that suppresses quantization noise within a given bandwidth around the desired output frequency.

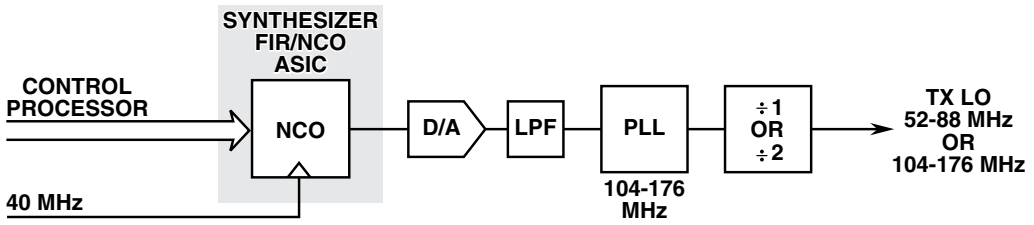

Figure 3-5 Transmit synthesizer circuit block diagram

The NCO output is converted to an analog signal by a D/A converter, filtered to remove alias components, and sent to the input of a conventional phase-locked-loop (PLL) frequency multiplier. The NCO output frequency range is in the 5.2- to 8.8-MHz range, and is multiplied by 10 or 18.5 for 52- to 88-MHz output frequencies, or 20 or 21 for 104- to 176-MHz output frequencies. A divide-by-two circuit provides the LO signal for operation in the 70-MHz band, and is bypassed for operation in the 140-MHz band. The PLL divider modulus of 20/21 is selected to avoid operating the NCO at output frequencies where there are large spurious signals close to the prime output. The choice of modulus is coded into the control software and is selected based on transmit frequency for optimum spurious performance.

Transmit IF stage

Modulator output must be amplified to the desired carrier level, and the level must remain stable through changes in frequency, temperature, time, and unit-to-unit component variation. Bandpass filtering is employed to limit out-of-band emissions (see figure 3-6).

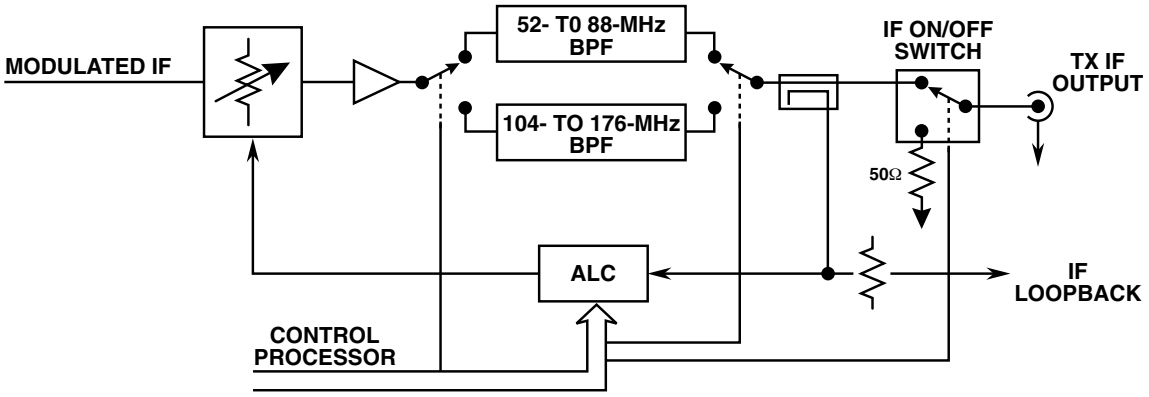

Figure 3-6 Transmit IF stage circuit block diagram

An automatic level control (ALC) loop maintains the transmit output power constant within tight tolerances.

The ALC loop functions as follows: the desired output power of the transmitter is set by a digital word from the control processor (CP). It is then converted to an analog reference voltage by a D/A converter. The output power of the transmit IF signal is converted to a DC level by an envelope detector and lowpass filter. This voltage is scaled, compared with the analog reference voltage, and the error between the two is amplified and used to control a voltage-controlled attenuator within the ALC loop. As the error of the ALC loop ultimately depends on the accuracy of the detector, the circuit has a maximum peak error of only 0.25 dB.

The power detector operates in either continuous or burst mode. In burst mode, the TX IF output is controlled by the transmit burst gate signal from the channel encoding section. ALC is not performed if the transmit burst gate indicates that no burst is being transmitted.

The detector accuracy and dynamic range is affected by forward bias drop of the detector diode. An automatic calibration circuit is included in the detector design which nulls out the imbalance under command from the control processor. A nulling voltage is derived from a D/A converter controlled by the CP. This voltage is adjusted until the zero-signal output of the detector nulls. The CP monitors the nulling process via an A/D converter connected between the detector output and the CP.

The control processor can either allow the ALC circuit to operate automatically or control the transmit level directly.

3.2

Receive operations

In the receive direction (see figure 3-1 on page 3–2), an IF signal is input at the IF IN connector on the IF panel, passed across the backplane, and received by the receive IF processor on the UMOD motherboard. The receive IF processor performs low-noise amplification, automatic gain control, and filtering. Once processed, the signal is routed to the receive synthesizer and demodulator, where the IF carrier is removed by either BPSK or QPSK demodulation. The resulting baseband data is then directed to the channel decoder where it is FEC decoded, differentially decoded, and descrambled. The data is then passed through the optional IFU daughtercard where deframing and other processing takes place.

The data is then routed to the receive portion of the terrestrial data interface daughtercard (either a data interface module or G.703 module). The interface module converts the receive data and clock to the appropriate formats, and directs the data across the backplane, which routes the signals to the CIM where they can be accessed by the user.

Backplane

The backplane serves as internal electrical interface between the IF IN port on the IF panel and ultimately the UMOD motherboard in any occupied chassis slot. Received IF signals are routed across the backplane to the UMOD motherboard. Once the receive data has been processed, the backplane routes data, control, and clock signals to the CIM.

Receive IF stage

The receive IF stage provides low-noise amplification (LNA), automatic gain control (AGC), and filtering of the received carrier (see figure 3-7).

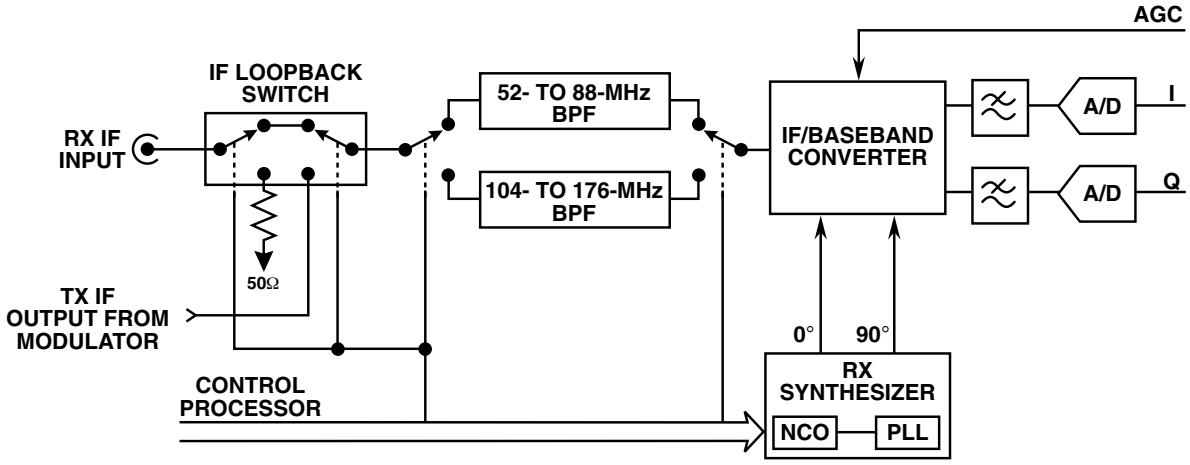

Figure 3-7 Receive IF stage and synthesizer circuit block diagram

The receive IF signal is bandpass-filtered to reject out-of-band signals. In-band signals accepted by the bandpass filters depend on the frequency (52-88 MHz or 104-176 MHz) the UMOD motherboard has been configured for. The filtered signal is downconverted (using a local oscillator, LO, derived from the receive synthesizer) to a second IF of either 20 MHz (52-88 band) or 40 MHz (104-176 band), lowpass filtered, and then sent sent through the AGC amplifier. AGC action, detected and controlled by the UDMOD ASIC, maintains the channel level constant at the input of the UDMOD ASIC. The signal is then converted to baseband by a quadrature downconverter. The resulting I and Q baseband signals are lowpass-filtered to remove the sum frequency components of the downconversion process, and to limit the bandwidth of the signals into the analog-to-digital (A/D) which prevents aliasing in converters that follow. The cutoff frequency of these lowpass filters is fixed and wide enough to pass the highest symbol rate signal (approximately 5 MHz). An additional signal monitor inside the RX FIR/NCO senses the output level of the quadrature downconverter to limit the power at that stage to avoid saturating the receive chain or the A/D converters.

The A/D converters digitize the I and Q signals to 8 bits and route the data to the I and Q inputs of the receive FIR/NCO ASIC.

Receive synthesizer

The receive synthesizer is similar to the transmit synthesizer with the main difference being that the synthesized frequency is either 20 or 40 MHz *above* the desired receive IF frequency, depending on the selected receive band of 70 or 140 MHz, respectively.

The VCO used in the synthesizer will tune from 144 to 216 MHz. LOs of 72 to 108 MHz are derived from the VCO output for tuning the 52 to 88 MHz band by a divide-by-2 output prescaler. In the 104 to 176 MHz band, the output prescaler is bypassed.

The receive transmit synthesizer PLL prescaler differs from the transmit synthesizer in that it is a divide-by-32/33 prescaler.

The PLL multiplies the output of an NCO to the final LO frequency range. The frequency resolution (Hz/LSB) of the Rx synthesizer is 0.15 Hz in the 140 MHz band and 0.075 Hz in the 70 MHz band, although it is limited to 1 Hz steps by the software.

Receive filtering

The digitized I and Q signals from the A/D converters are processed by the receive FIR/NCO ASIC as follows: First, the digitized samples are multiplied by sine and cosine digital sinusoids whose frequency and phase are controlled by the output of the carrier recovery loop (CRL) filter. Next, the signals are decimation-filtered to reduce the sample rate from the 10- to 20-MHz range to 4 samples/symbol (see figure 3-8). The decimated signals are sent through FIR filters, whose impulse response is programmable and is typically arranged so that the transmit FIR and receive FIR filters form a matched filter pair (square-root raised cosine, for example). Finally, a decimation-by-2 is performed on the filter output to produce I and Q 2-sample/symbol output sequences that are passed on to the demodulator.

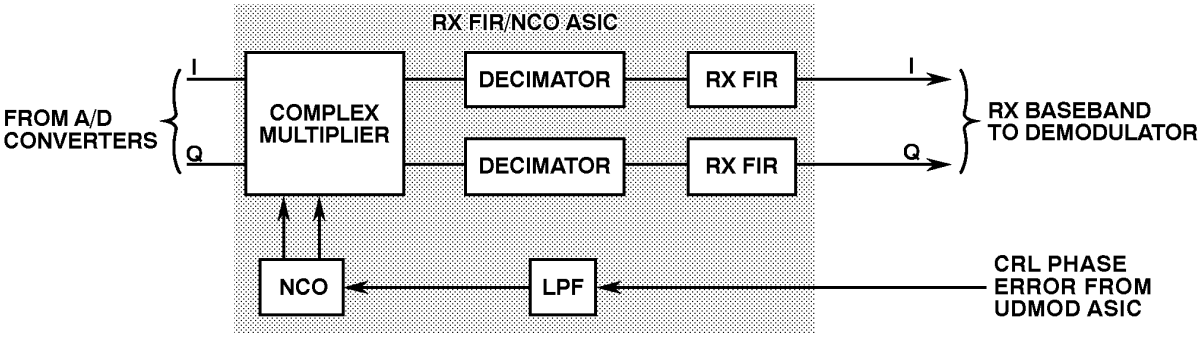

Figure 3-8 Receive filtering circuit block diagram

The FIR/NCO and A/D converter both use the same clock so that sampling of the signal and processing by the FIR/NCO and demodulator ASICs are synchronous. The clock signal into the demodulator ASIC is provided by the FIR/NCO as a byproduct of the sample rate decimation process.

Demodulator

Signal demodulation is performed by the UDMOD ASIC (see figure 3-9). The signal is processed by many sidechains which perform the functions of:

- Carrier recovery phase error detection
- Bit timing recovery (BTR)
- Receive power detection and AGC control
- Acquisition sweep control
- E_s/N_o determination

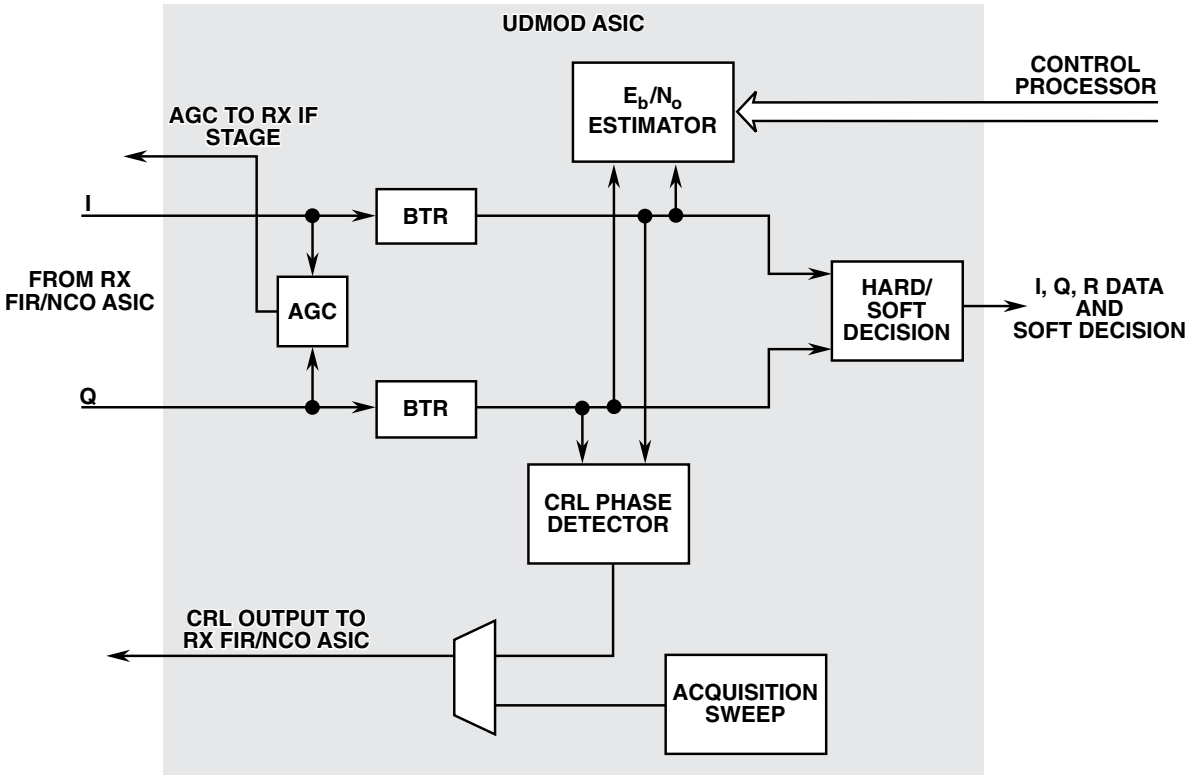

Figure 3-9 Demodulator circuit block diagram

CRL loop filtering is performed in the receive FIR/NCO ASIC. AGC filtering takes place in a digital filter in the UDMOD ASIC.

The output of the demodulator is I and Q demodulated data at the transmitted symbol rate, each quantized to one sign bit and two magnitude bits. Soft-decision mapping is configurable for BPSK and QPSK operation.

Channel decoding

The channel decoding section of the UMOD motherboard is responsible for formatting the data after it has been demodulated.

The decoding circuitry (see figure 3-10) performs the functions specified in IESS-308 (IDR) and IESS-309 (IBS) that relate to forward error correction and descrambling.

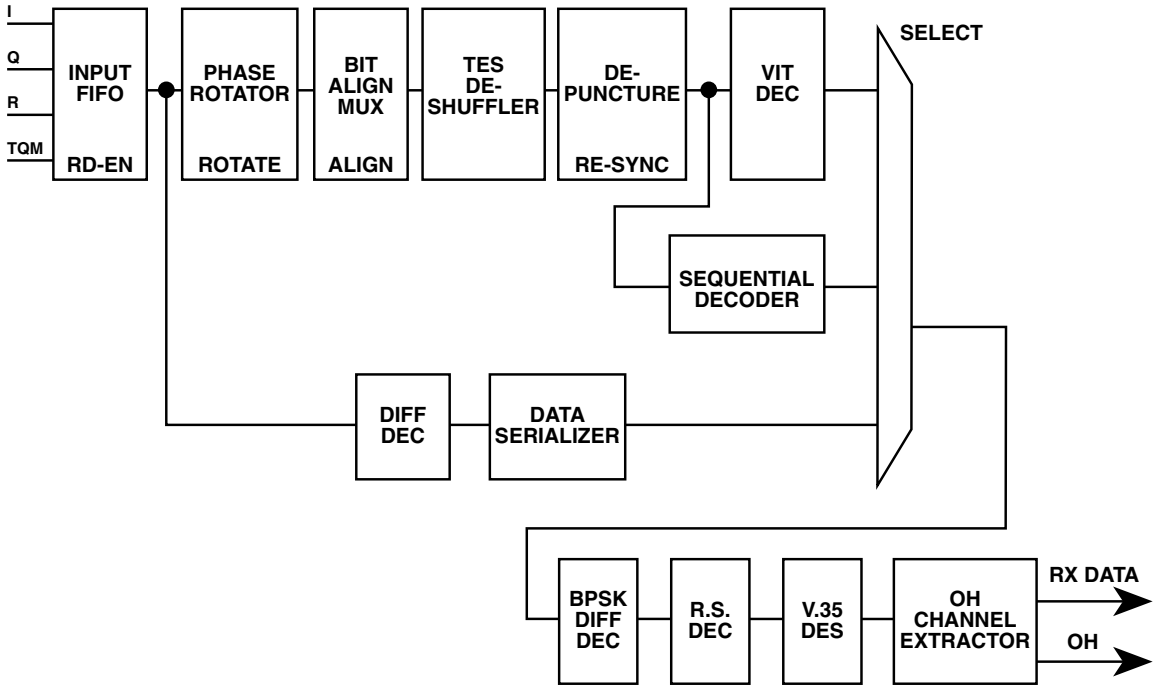

Figure 3-10 Channel decoding circuit block diagram

The channel coding circuit performs the following functions:

- Descrambling data for energy dispersion purposes
- Differential decoding for resolution of phase ambiguity in the demodulator during initial acquisition and following cycle slips
- [Detecting the Overhead Channel Frame Marker and extracting the data packet]
- Converting FEC Rate 1/2 to Rate 3/4 or Rate 7/8 (Puncturing)
- Viterbi Decoding

Text inside of brackets—[ ]—denotes features currently under development.

- Reed-Solomon decoding
- De-interleaving for use with Reed-Solomon decoding
- Concatenated Viterbi/Reed-Solomon decoding

The encoding circuit operates in the following modes:

- BPSK—Rate 1 (no FEC); Rates 1/2, 3/4, and 7/8 Viterbi only; Rate 1/2 Sequential only; Rates 1/2, and 3/4 with Viterbi and Reed-Solomon concatenated
- QPSK—Rate 1; Rates 1/2, 3/4, and 7/8 Viterbi only; Rate 1/2 Sequential only; Rates 1/2, and 3/4 with Viterbi and Reed-Solomon concatenated

Channel decoding interfaces

The data interface between the demodulator and the channel decoding circuit consists of two channels: I and Q. Each channel has a parallel 3-bit sign magnitude format, or two channels each having a parallel 6-bit/symbol format for BPSK/QPSK operation. Soft-decision symbol data is clocked into the receive channel coding from the demodulator, processed and then passed in serial format either to the framing unit or directly to the terrestial port. Muliplexing of the transmit and receive data paths to and from the internal framing unit or the terrestial interface is under software control.

Descrambling

Data descrambling performs the complementary operation associated with the distant scrambler. Two types of descramblers are provided: V.35 and IESS-309 (IBS).

The V.35 descrambler used when operating within an IDR or TES network is self-synchronizing and meets CCITT V.35 specifications. The descrambler is reset to a known state between bursts and is enabled during a burst.

The IESS-309 descrambler is selected when the UMOD is operating in an IBS network. The descrambler will self-synchronize upon receiving a sequence of 001001001001001.

Differential decoding

The channel decoding section supports both BPSK and QPSK differential decoding. When BPSK modulation is used, the BPSK differential encoder and BPSK differential decoder resolve 180-degree phase ambiguity in the received data when a demodulator carrier cycle slip causes inversion of the data. Because the Viterbi decoder will decode and correct errors but produce inverted data in such an event, biphase differential coding is required. In the case of QPSK modulation the QPSK encoder and decoder resolve 90-degree phase ambiquity. The selection of differential coding type is software controlled. In addition,

differential coding may be bypassed when not required. QPSK differential decoding is used only in R1 QPSK. The BPSK differential decoder is used for R1 BPSK, and when FEC is enabled.

Forward error correction decoding

The following is a list of the forward error correction (FEC) decoding methods supported by the channel decoding section:

- Rate 1/2, 3/4, and 7/8 Viterbi decoding
- Rate 1/2 Sequential decoding using the Sequential decoder
- Rate 1/2 and 3/4 concatenated Viterbi and Reed-Solomon
- De-interleaving when Reed-Solomon is selected

TES deshuffler

This circuit is included as part of the UMOD channel coding to allow compatible operation within a TES network.

Demodulator interface (preamble and postamble extraction)

This circuit is included as part of the UMOD channel decoding to allow compatible operation within a TES network.

Internal framing unit (IFU)

The IFU buffers received data for plesiochronous operation or to negate Doppler-related timing problems caused by satellite motion; supports Engineering Service Channel (ESC) supervisory overhead; and provides backward alarm functions.

IDR mode

In a standard framing operation, receive data enters the IFU from the UMOD motherboard. The IFU deframes the data, removes ESC supervisory information from the data, descrambles it, and then outputs the signals to the terrestrial data interface daughtercard (either a DIM or GIM).

For a D&I operation, frames enter the IFU from the UMOD motherboard. The IFU removes ESC supervisory information from the frames, descrambles them, inserts the frames into preselected timeslots on the bearer, then outputs the frames to the terrestrial data interface daughtercard (either a DIM or GIM).

IBS/SMS mode

In a standard framing operation, receive data enters the IFU from the UMOD motherboard. The IFU removes ESC supervisory

information from the data, descrambles it, and then outputs the signals to the terrestrial data interface daughtercard.

For a D&I operation, frames enter the IFU from the UMOD motherboard. The IFU removes ESC supervisory information from the frames, descrambles them, and then outputs the frames to the terrestrial data interface daughtercard.

For more information on the IFU daughtercard, refer to section 3.7 on page 3–51, “Internal framing unit daughtercard.”

Overhead channel

A user–definable overhead channel is available for closed network applications. See appendix H for details.

Terrestrial data interface

The terrestrial data interface daughtercard (installed on the UMOD motherboard) converts the TTL-level data from the UMOD motherboard to the baseband data interface format required by the user DTE device. There are two types of data interface daughtercards:

- Data interface module (DIM)
- G.703 interface module (GIM)

DIM

The DIM takes receive data from the UMOD, converts the TTL level data and clock signals from the UMOD motherboard into one of the following electrical formats: EIA RS-232, EIA RS-422/449, or CCITT V.35.

For more information on the DIM daughtercard, refer to section 3.6 on page 3–41, “Terrestrial data interface daughtercard.”

GIM

The GIM performs HDB3/B8ZS/B6ZS line coding on data received from the UMOD. It converts the data from TTL to the required G.703 format, and then outputs the resulting data to the user’s DTE device.

The GIM supports two bipolar baseband interfaces. The first (or *main*) interface is used by the UMOD for interfacing with the user DTE device and is capable of operating with mixed T1 (balanced), E1 (balanced or unbalanced), T2 (balanced or unbalanced), and E2 (unbalanced) transmit and receive data rates.

The second bipolar interface, along with the main bipolar interface, support twin-bearer D&I multiplexing. This function uses the DDO (drop-data-out) and IDI (insert-data-in) ports on the CIM. The IDI port is used with the RD (outgoing) port on the CIM to provide the insert multiplexer, and the DDO port is used with the SD (incoming) port to provide the drop multiplexer. Normally

both D&I multiplexers are operate at the same rate, however, the GIM is designed to allow for a mixed-rate operation. For example, the user can set up the drop multiplexer (SD and DDO ports) to operate in T1 mode, and the insert multiplexer (RD and IDI ports) to operate in E1 mode. For E1 operation a mixture of balanced and unbalanced interfaces is allowed. The selection of one of the appropriate coding schemes (AMI, B8ZS, or HDB3) is independent for every port.

For more information on the GIM daughtercard, refer to section 3.6 on page 3–41, "Terrestrial data interface daughtercard."

Customer interface module

The CIM is the interface between the UMOD and the user's equipment. Receive data from the UMOD can be output to the user DTE device in the following electrical interface formats.

- EIA RS-232, EIA RS-422/449, or CCITT V.35. These formats are supported by the 37-pin connector labeled *TO DTE*.
- CCITT G.703. This format supports balanced T1 (also called DS1), balanced or unbalanced E1 (also called CEPT), balanced or unbalanced T2 (also referred to as DS2), and unbalanced E2 electrical interfaces. The balanced G.703 port is labeled *G.703 BAL*, the unbalanced G.703 ports are labeled *SD* (send data) and *RD* (receive data).

The CIM provides ports for drop-and-insert (D&I) multiplexing and a port for Engineering Service Channel (ESC) signals for use with an optional internal framing unit (IFU). The D&I ports on the CIM are labeled *SD* (send data), *RD* (receive data), *IDI* (insert-data-in) and *DDO* (drop-data-out). ESC signals (including audio ESC, octet alignment, and backward alarms) are supported by the CIM port labeled *ESC SIGNALS*.

The CIM also has a station clock port (labeled *STATION CLK*) that can receive a 1 MHz to10 MHz TTL or 0 dBm to +25 dBm level input.

System functions

System functions support the receive and transmit functions, and provide means for controlling, monitoring, and testing the UMOD. The functions include:

- Control processor (CP). The CP is responsible for UMOD control and status monitoring, as well as data transport in the case of asynchronous baseband data.
- Timing generator. The timing generator is a DDS-based multifrequency synthesizer that is responsible for generating the many clock signals required by the UMOD.
- Redundancy option. The redundancy option protects against communications disruptions by automatically replacing a failed primary UMOD with a redundant unit.
- Bit error rate tester (BERT). BERT enables simple troubleshooting of the satellite network parameters without requiring sophisticated test equipment. The BERT function consists of an independent transmit pattern generator and a receive error analyzer. For more information on the BERT, refer to chapter 3.8 on page 3–63, “Loopback tests and bit error rate tester functions.”

Control processor

The UMOD operator uses software commands to set UMOD parameters. The CP translates the configuration information into commands understood by UMOD circuitry. The control processor is responsible for initializing UMOD components after a reset, loading UMOD applications software, performing startup diagnostics, performing logic functions required for call processing, and participating in network management and control. The CP controls data port data rates, multidrop port direction, and baseband data modem control signals. In addition, the CP controls and monitors the following UMOD components:

- Modulator. The CP sets the transmit modulation type (BPSK or QPSK); controls the loopback mode; enables the IF output; controls output power; and monitors for failure conditions.
- Demodulator. The CP monitors demodulator status, receive power level, frequency offset, and coarse E_b/N_o. The CP also sets the receive demodulation type (BPSK or QPSK) and controls the receive symbol rate.
- Frequency synthesizer. The CP controls transmit and receive IF frequencies, and monitors lock status.
- Timing generator. The CP controls the UMOD timing configuration (internal, external, or loop); sets the transmit and receive data and symbol rates; and controls the coding and framing rates.
- Channel coding section. The CP enables and controls the FEC type selection (Viterbi, Reed-Solomon, Sequential, Concatenated), scrambler/descrambler type selection (V.35

and IESS-308), and differential encoder/decoder type selection (BPSK, QPSK).

- Internal framing unit. The CP controls IDR/IBS mode selection, ESC audio/64-Kb data selection, and monitors frame synchronization.
- Doppler buffer. The CP enables the Doppler buffer; sets the buffer depth; and monitors buffer fill status for overflow or underflow conditions.
- Bit error rate test circuit. The CP selects the pattern used during a BERT; sets the block length; controls the insertion of errors; selects the synchronization threshold; and monitors the bit error rate (BER).

The CP also controls the light-emitting diodes (LEDs) on the UMOD motherboard; monitors chassis address code and chassis type information; controls the summary alarm relay; and monitors slot ID code information.

The core of the CP is a microprocessor operating at 16 MHz (see figure 3-11). The CP has 128 Kbytes of programmable read-only memory (PROM) for TES-mode boot code memory, another 64-Kbyte PROM for UMOD-mode boot code memory, 256 Kbytes of flash memory, 448 Kbytes of pseudo-static random-access memory (PSRAM) and 8 Kbytes of electrically-erasable programmable read-only memory (EEPROM). UMOD operational code resides in the flash memory while TES mode operational code is downloaded into PSRAM. Non-volatile parameters reside in EEPROM.

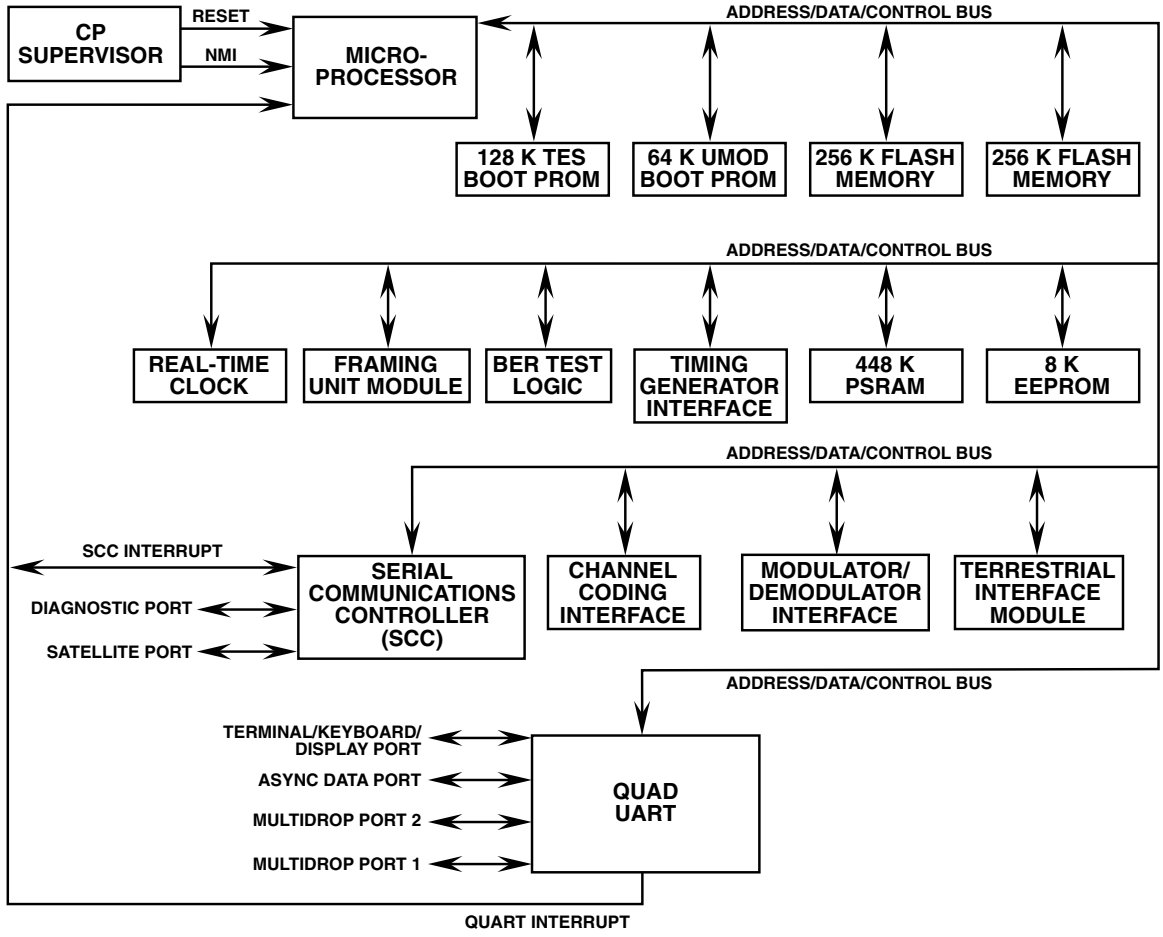

Figure 3-11 Control processor block diagram

Timing generator description

The timing generator (TGEN) provides all clock signals used on the UMOD module other than processor and baud rate clocks. The timing generator consists of a transmit timing generator (TXTG) and a receive timing generator (RXTG).

Transmit timing generator

Figure 3-12 is a block diagram of the transmit timing generator. The TXTG provides the following clock signals:

- Transmit information rate clock (user rate)
- Transmit information rate
- Framing unit overhead clock
- Transmit overhead channel rate clock (information rate x 256/255)
- Transmit Viterbi encoding symbol rate
- Transmit Reed-Solomon encoding symbol rate

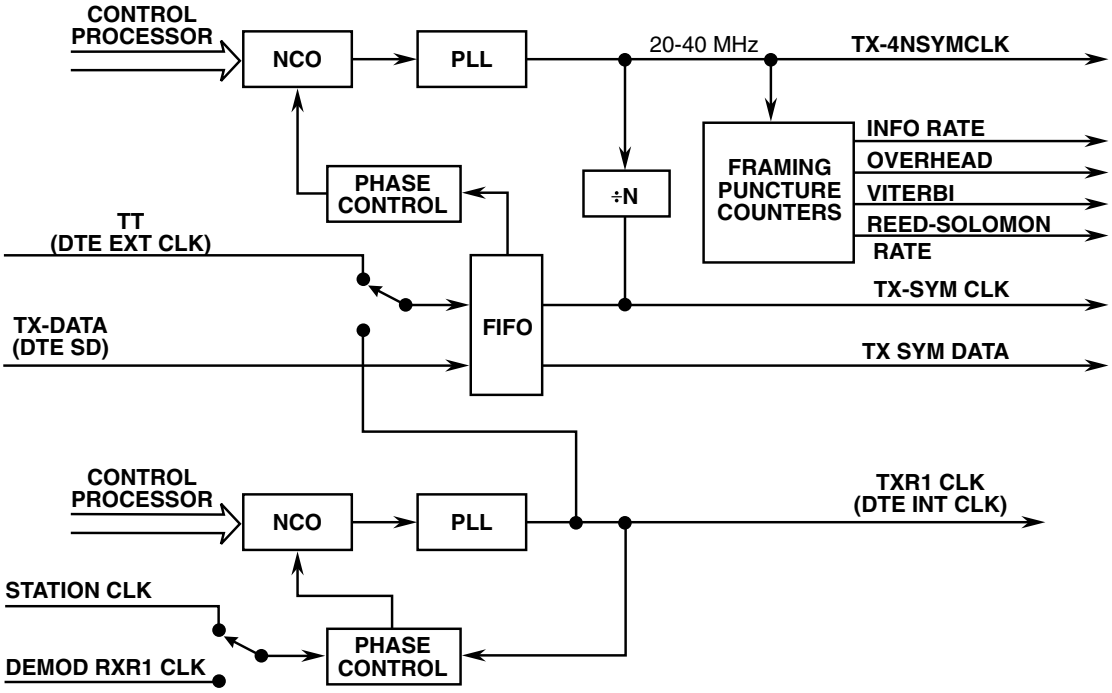

Figure 3-12 Transmit timing generator block diagram

Transmit clock signals are generated by a programmable sequencer that punctures a clock sourced by a numerically-controlled oscillator (NCO). The TXTG receives its reference clock from a reference oscillator. When the TXTG locks onto an external reference clock, a digital phase-locked loop (PLL) is enabled with the selected reference, maintained by correction values that the CP inputs to the NCO.

The transmit timing generator reference frequency is selectable from one of the following three sources:

- Internal 10-MHz TCXO clock
- Receive symbol clock (if loop timing is being used)

- External clock—The transmit timing generator is phase locked to a user supplied clock (either a terrestrial data clock or a station clock).

Receive timing generator

Figure 3-13 is a block diagram of the receive timing generator. The RXTG provides the following clocks signals:

- Receive overhead channel rate clock (information rate x 256/255)
- Receive Viterbi encoding symbol rate
- Receive Reed-Solomon encoding symbol rate
- Receive information
- Framing overhead clock
- Demodulator clock

RXTG operation is identical to the TXTG. The clock signals are generated by a programmable sequencer that punctures a high-speed clock sourced by an NCO. The NCO output clock frequency is programmable through its CP interface. The RXTG receives its reference clock from a highly-stable reference oscillator and is phase-locked to the recovered symbol clock from the demodulator. A digital PLL, wherein the CP calculates and inputs correction values to the NCO, is used to maintain lock with the recovered clock.

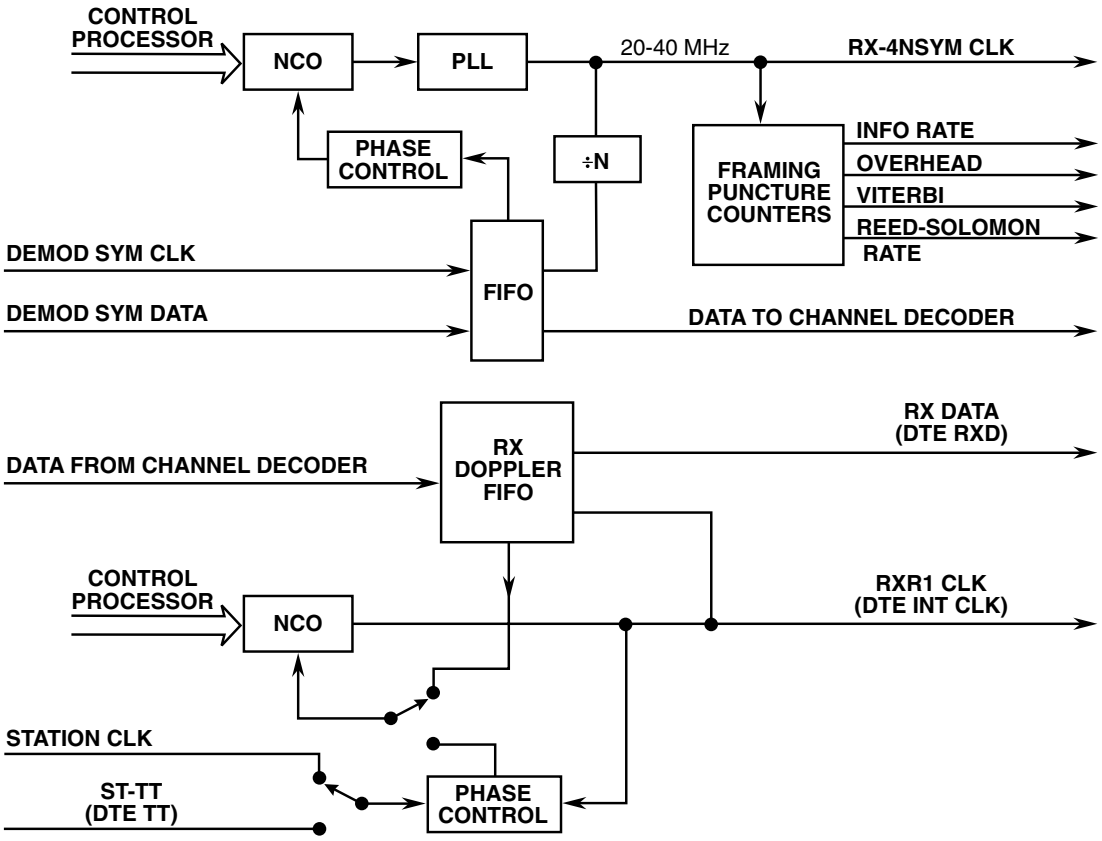

Figure 3-13 Receive timing generator block diagram

The receive timing generator reference frequency is selectable from one of the following sources:

- Satellite clock (recovered symbol clock)
- External clock—The receive timing generator is phase-locked to a user-supplied clock which can be either a terrestrial data clock or a station clock

Monitor and control description

This section describes the Universal Modem monitor and control (M&C) feature that is used to configure the UMOD for operation. The M&C feature provides the following:

- General configuration controls. These provide the user with options to modify routine settings on the UMOD (for example, setting the modem's mode of operation, setting the date and time, configuring the modem to automatically restart after a power cycle, etc.).
- Terrestrial interface configuration controls. These enable the user to configure the data interface module (DIM) or the G.703 interface module (GIM).
- Modem configuration controls. These functions allow the user to configure modem settings for data rate, transmit and receive frequencies, modulation and filter types, transmit power level, etc.
- Channel coding configuration controls. These allow the user to configure modem settings for transmit and receive differential coding, transmit and receive scrambling, the FEC rate and type, etc.
- Modem control and configuration controls. These control such modem functions as activating the transmit carrier, resetting the modem, enabling the overhead channel, determining whether the front panel or the terminal interface will control the quad universal asynchronous receiver/transmitter (QUART) channel, and configuring the modem to install software into flash memory.
- Diagnostics controls. The Universal Modem has built-in diagnostics that can verify functioning of the LED and audible alarm, perform internal loopback tests, and run bit error rate tests (BERT).
- Status retrieval controls. These enable the user to display the status of the satellite link, the terrestrial interface, the modulator, the demodulator, the encoder, the decoder, or the redundant modem.
- Local Alarm Reporting Mechanism. This feature reports alarm conditions that may arise in the near Universal Modem.

The 9100 Universal Modem provides two user interfaces (see figure 3-14) for controlling and configuring UMOD features:

- Front panel keypad/display (available on the 1-PAK chassis only).
- Terminal interface. An ASCII terminal or IBM PC-compatible computer can connect to the UMOD terminal interface port located on the CIM. The port—labeled *M&C*—enables the user to configure and monitor the UMOD using built-in terminal software or the optional Windows-based M&C software.

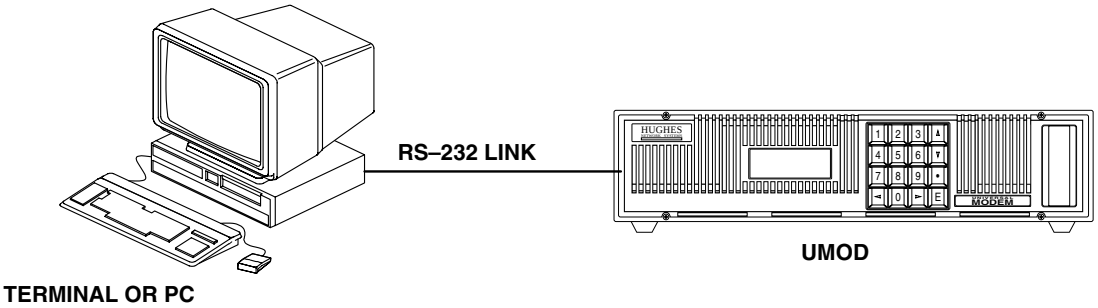

Figure 3-14 Controlling the UMOD via the terminal interface

In addition, commands and responses can be communicated between modems using the multidrop interface and satellite overhead channel.

UMOD 1-PAK chassis front panel keypad/display

The UMOD 1-PAK chassis front panel keypad/display (see figure 3-15) provides the user with command, control, and monitoring capabilities without requiring a remote control unit. In situations where an ASCII terminal or PC-compatible computer is not available, the control panel provides access to the UMOD to configure or monitor UMOD functions.

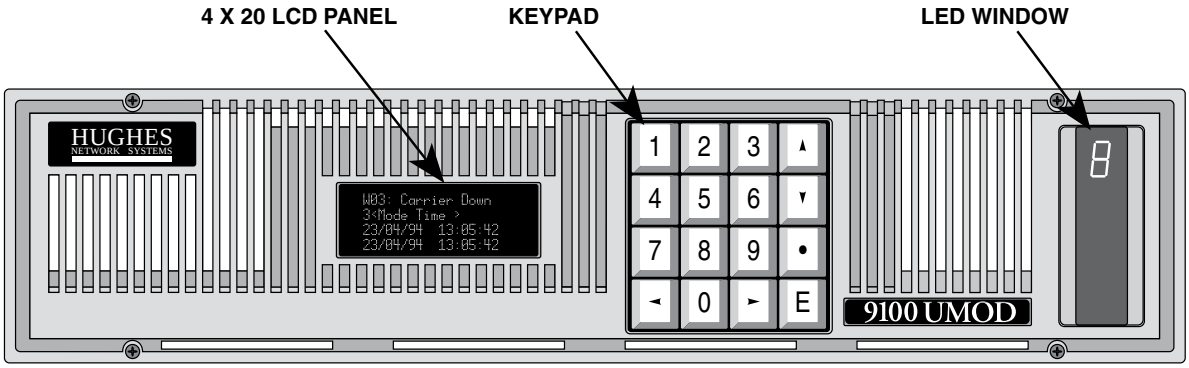

Figure 3-15 1-PAK chassis front panel

The front panel consists of a 16-key keypad, a 4x20-character liquid-crystal display (LCD) panel and a light-emitting diode (LED) window. The LCD panel and LED window can display status and fault messages, enabling the operator to scan the modem for abnormal operating conditions.

Front panel keypad operation

The front panel provides access to commands that control the UMOD. Some commands are used to modify parameters, others display operating parameters. These commands are organized in a structure of menus and lists of commands as illustrated in figures 3-16 on page 3–32 and 3-17 on page 3–33. The complete list of panel commands is provided in appendix B. You enter information using the keypad to scroll through menus and lists of commands, and by making the appropriate selections or entries. A slowly blinking cursor identifies the selection or formatted space to enter data.

LCD panel display

The top line of the LCD panel display is reserved for system events and alarms. Note that following a power–on action, “I02:Power Up” displays on the top line and the main menu is displayed on the next three lines.

LCD panel main menu

The main menu as illustrated in figure 3-16 displays when the UMOD power is turned on or when selected during the display of another menu or command/status message.

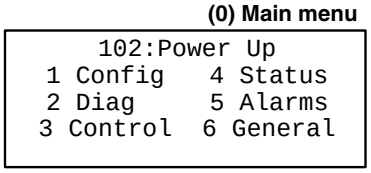

Figure 3-16 Main menu following power–on procedure

Navigating LCD panel menus and command/status displays

1. Using the structure illustrated in figure 3-17 on page 3–33 as a guide in navigating to a command, start with the main menu and select an item by pressing the keypad key (**1** through **6**) corresponding to the item number in the illustration.

   The related menu (Config menu for example) will display with a list of selections which, when selected by pressing a keypad key, will display either a sub menu or a command.

   - If a menu displays, select an item with the keypad in the same manner as with the main menu.
   - When a command displays, it will also display its current value on the next line which is updated every 2 seconds (until you press the **E** key to stop the updating). The last line is formatted with values to select with the cursor (controlled by the ▶ and ◀ keys) or with space to enter values via the keypad. A > symbol at the right of the parameters to be selected indicates that more parameters are listed; use the ▶ key to display the hidden parameters. A < symbol to the left of the parameters indicates hidden parameters that can be viewed by pressing the ◀ key.

     Enter the cursor–selected or keypad–entered data by pressing the **E** keypad key.
2. To select other commands within the same list, press the ▼ or ▲ keys.
3. To return from a command to its menu, step through the commands with the ▲ or ▼ keys until the menu displays.
4. To return to the next higher level menu from a menu, press the **9** key.
5. To return to the main menu from any menu, press the **0** key.

Note

The decimal point (**.**) key is not functional in the current version.

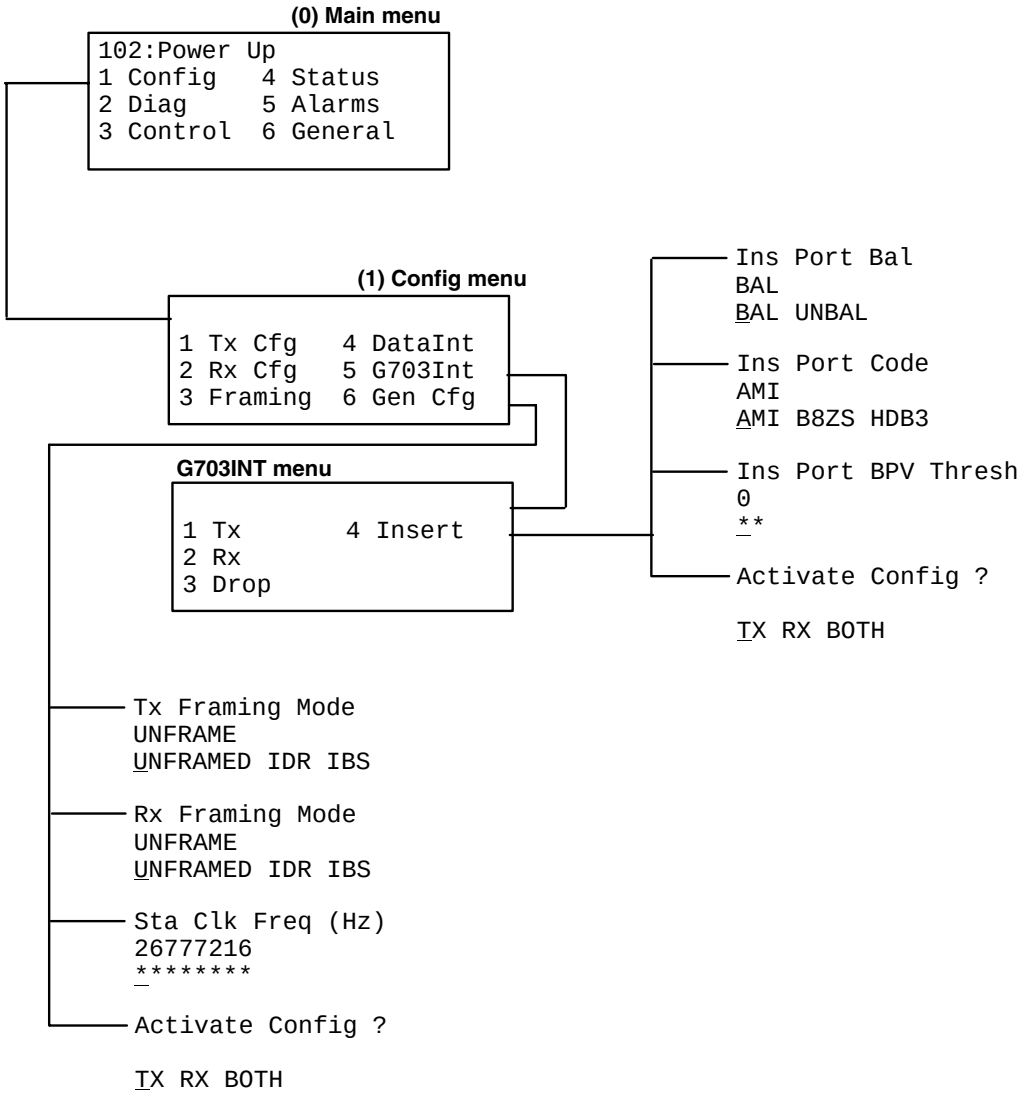

Figure 3-17 Configure G703Int & Gen Cfg panel commands

Terminal software

If an ASCII terminal is being used, the user accesses the M&C using mnemonic commands typed in at the ASCII terminal keyboard. For example, to set the transmit modulation (TM) command for BPSK operation, the user would type:

<TM B

This type of access is called a command line interface, or CLI. A summary of the terminal commands is provided in Appendix C,

and the M&C configuration commands are provided in Appendix D.

Windows-based UMOD M&C software

The Windows-based UMOD M&C software runs in Microsoft Windows, a graphical user interface (GUI). Windows applications are much easier to use than a CLI because the operator uses a mouse to select descriptive terms instead of hard-to-remember mnemonic codes. Once the user has selected a command, the UMOD M&C software translates that command into the appropriate terminal command understood by the Universal Modem.

For example, to set the transmit modulation (TM) command for BPSK operation in the UMOD M&C software, the user would use the mouse to select the *UMOD Configuration* menu (see figure 3-18 on page 3–34), click on the *Modulation Type* pull-down menu button (showing QPSK), and select BPSK.

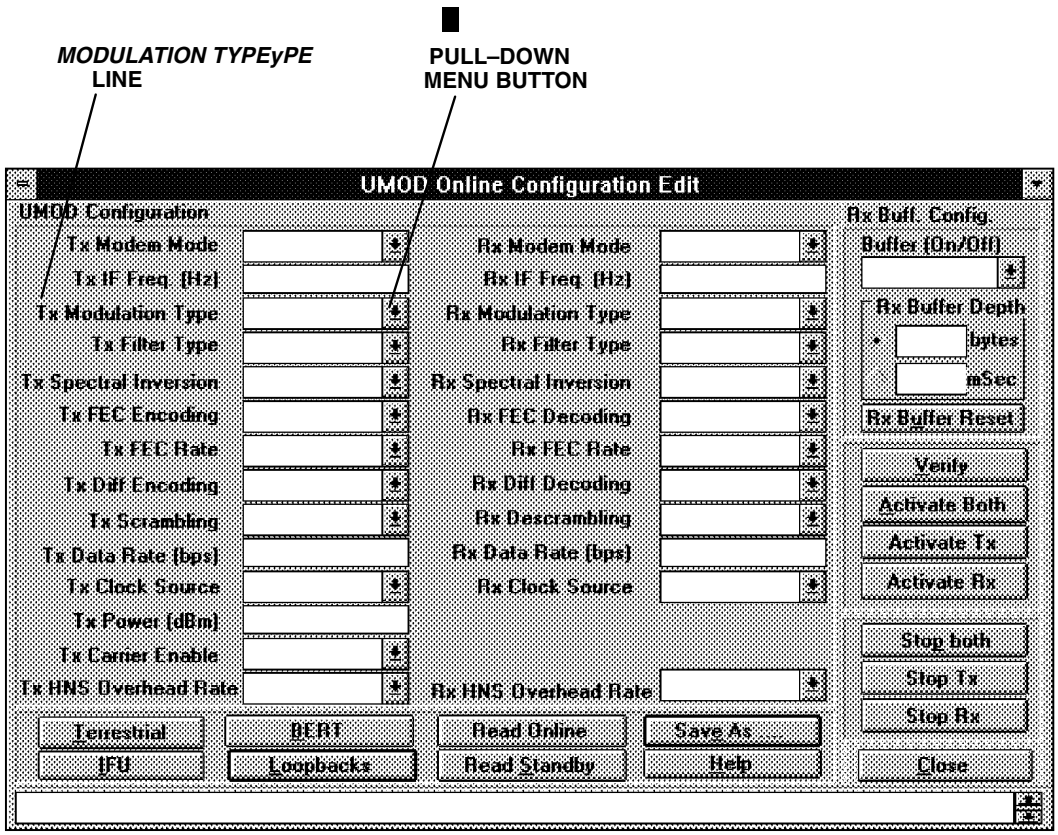

Figure 3-18 Selecting the modulation type using the M&C software

Inter-UMOD M&C communication

There are two ways to control a single UMOD: through an ASCII terminal or PC connected to the terminal interface. Often, however, it is useful to control several modems from a single control point. This section describes how inter-UMOD communications are achieved.

The possible connection paths are shown in figure 3-19. The ASCII terminal or PC is connected by an RS-232 serial link to a single UMOD with which it can communicate. In addition, all the modems in a single chassis are inter-connected by an RS-485 multidrop link. The multidrop link enables the ASCII terminal/PC to control any modem in the chassis. Multiple chassis can also be connected to the same multidrop link, provided the bottom 15 bits of the chassis ID code are the same. The terminal/PC can control up to 30 modems through the single physical connection.

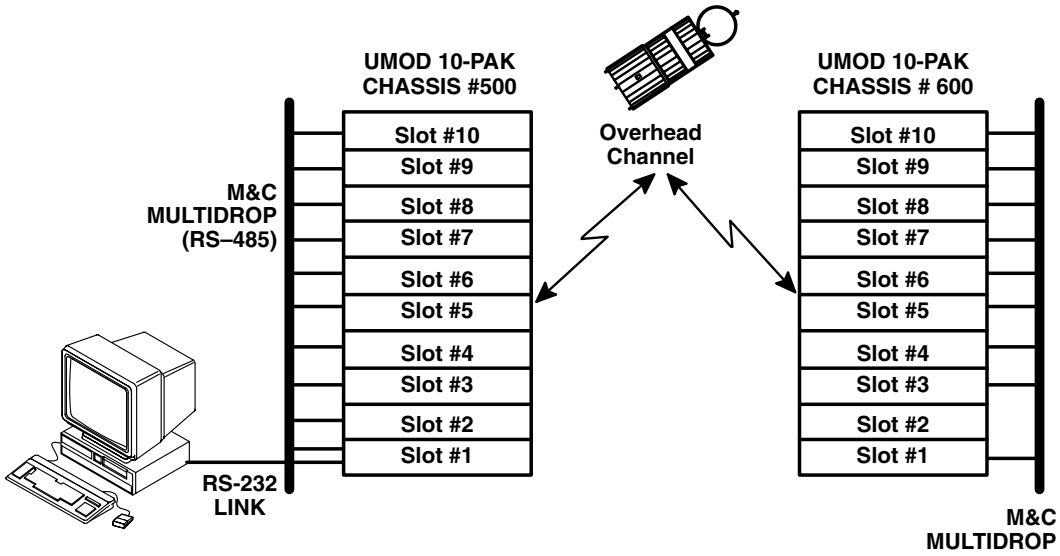

Figure 3-19 Inter-UMOD communications paths

In a closed network, besides controlling the modems at the near site through the multidrop link, it is also possible to control far modems via satellite. When UMODs are connected using one of the Hughes Network Systems, Inc. communications formats, a user selectable overhead channel (OHC) may be added to the user data, through which the far UMOD can be controlled by the near terminal/PC connection. The overhead channel facility cannot be used in open networks (such as IDR/IBS), or if a modem other than a UMOD is part of the connection.

Text inside of brackets—[ ]—denotes features currently under development.

M&C multidrop interface

Figure 3-20 shows the multidrop connection. All modems operate independently (in other words, there is no master or slave).

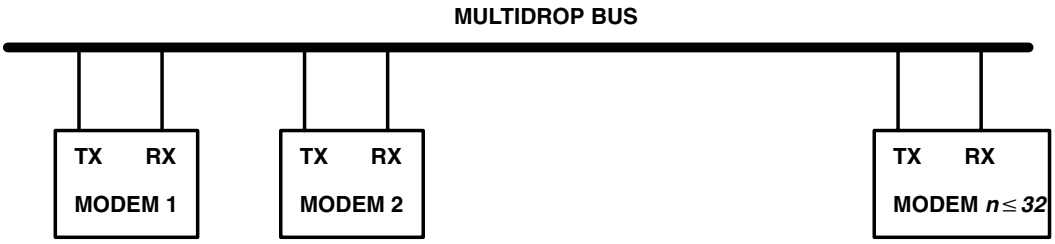

Figure 3-20 Multidrop bus

On the multidrop bus, a transmit frame can be received by all modems, including the originating modem. This broadcast feature enables the originator to verify whether or not the transmission is corrupted. A modem preparing to transmit will check the bus for traffic before sending, if the bus is already in use, the transmission will be retried after a random delay.

The modem initiating the transmission controls the multidrop bus until the message is entirely transmitted. Each frame is protected by a one-byte checksum to guarantee data integrity. If more than one UMOD tries to transmit a frame at the same time or within a very close interval, the data will be corrupted and thus discarded by the receiving UMODs.

Traffic contention on the multidrop bus

Access to the multidrop bus is contention-based. That is, every modem has equal access to the bus. Contention occurs when two modems want to transmit a message at the same time. Using a protocol similar to the Ethernet Carrier Sense Multiple Access/Collision Detection (CSMA/CD) helps avoid most contention problems on the multidrop bus. CSMA/CD protocol does the following:

- It causes the sender to listen for traffic before transmitting, and to transmit only when no other UMOD is transmitting.
- During a transmission the sender will listen for data collisions, abort transmission if they occur, and reschedule the transmission.

Redundancy option

The 9100 UMOD provides an optional redundancy feature that allows one UMOD motherboard to be reserved as a spare for *n* operational UMODs (where n is selected from 1 through 8). This feature enables the user to avoid communications disruptions caused by the failure of a UMOD.

The spare UMOD maintains a copy of the operating configuration for each of the online (primary) UMODs over which it has control. This is accomplished by polling all of the primary UMODs in the redundant domain.

A failure is signalled to the redundant UMODs when a hardware line is set to a failed state. The redundant UMOD motherboard then switches the user terrestrial interface lines to itself, and begins operating in whatever mode the primary UMOD was in previously.

The redundant modem also polls each of the primary UMODs for their status. Status indications of an ongoing or incipient failure in a primary UMOD is also sufficient for the redundant UMOD to switch in.

Redundancy using a 1-PAK chassis

Two 1-PAK chassis may be set up to be 1:1 redundant (see figure 3-21). A redundancy cable connects the redundant 1-PAK chassis to the primary 1-PAK chassis (a multidrop cable is also connected between the chassis).

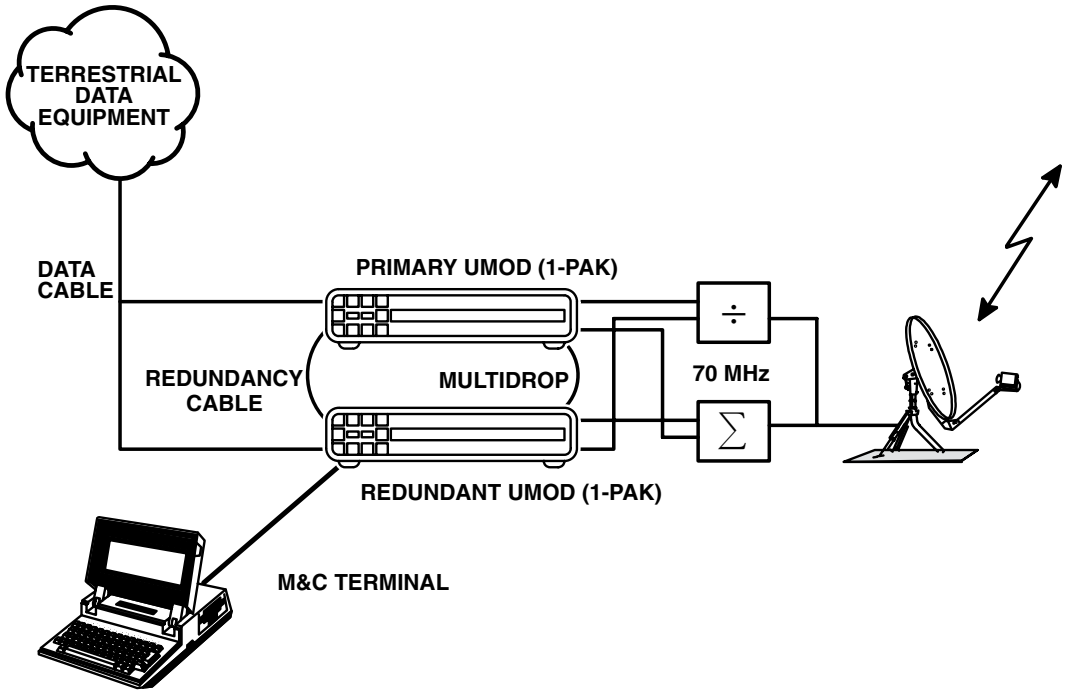

Figure 3-21 1-PAK chassis 1:1 redundancy

The redundant modem is inhibited from transmitting until it takes active control from the failed primary modem. However, to speed acquisition during a switchover, the redundant modem will use the frequency offset information collected during polling to assist its acquisition.

Detecting primary modem failures

Each of the primary modems has a modem failure status line leading from it to the redundant modem. The redundant modem checks these lines every 16 ms to determine whether any of the primary modems has failed. If a UMOD has failed, the redundant modem will then switch in for the failed primary as long as the redundant modem is not already switched in for another primary UMOD.

Redundancy polling

The redundant UMOD periodically polls all of the primary modems in its domain to verify that none of the primary units have failed (see figure 3-22).

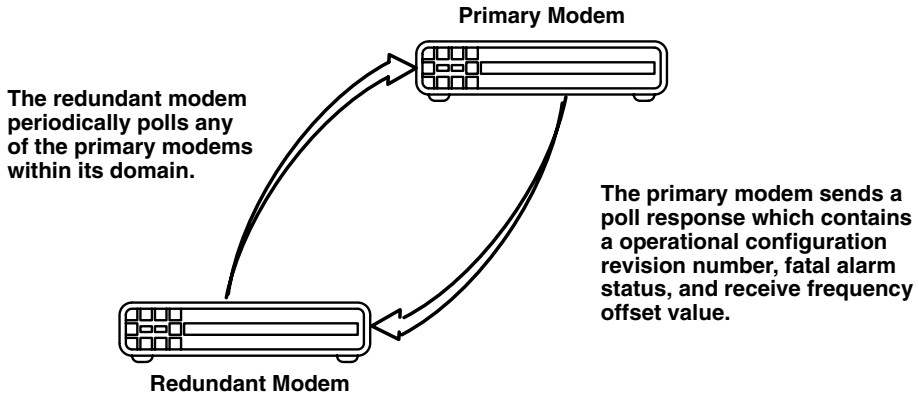

Figure 3-22 Redundancy poll-response

The poll response data consists of a configuration revision number, frequency offset, and status indicators for the given primary unit.

The polls enable the redundant modem to monitor for fatal alarms on the primary units. The polls also allow the redundant modem to maintain a copy of the current primary modem receive frequency offset to reduce acquisition time if a switchover occurs.

When the redundant UMOD receives a configuration update from a primary modem, it copies the data to the appropriate redundancy storage profile; each storage profile in the redundant modem corresponds to a specific primary modem (see figure 3-23 on page 3–39).

Each redundancy storage profile contains primary modem operating configurations, such as receive frequency offset, operating configuration level, service state (operational or failed), and missed poll count. These values are stored in memory and are updated each time a poll response is received from the primary UMOD.

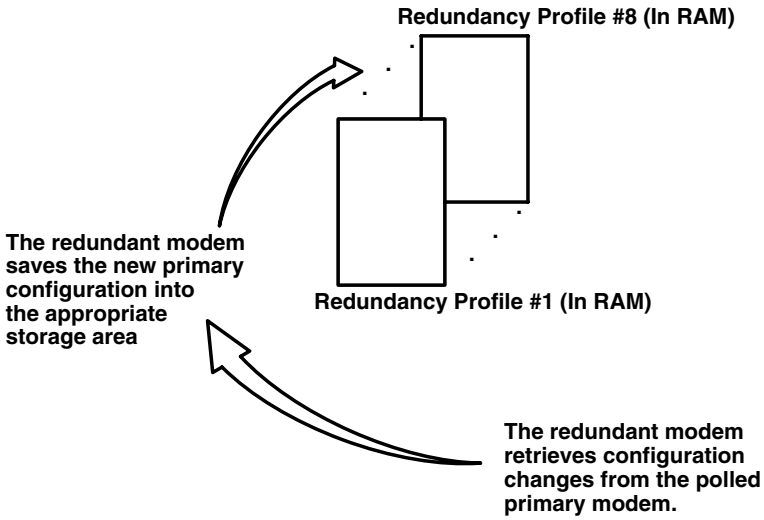

Figure 3-23 Redundancy configuration management

How the UMOD handles a primary modem failure

If a primary modem detects an internal fatal error, it will notify the redundant UMOD that it has failed and sound the audible alarm to alert an operator.

The failed primary UMOD will automatically cease transmission. This will occur whether or not redundancy is being used. The failed UMOD will reject any commands to enter operational mode, and will display a failure code on the front panel LED window/terminal display.

At this stage, if the UMOD chassis has been configured for redundancy protection, the redundancy switchover can either take place automatically (without waiting for operator intervention), or the switchover can be controlled manually.

Automatic switchover

If the redundant UMOD has been configured to automatically switch over, the criteria for switching from the primary UMOD to the redundant are as follows:

- The redundant UMOD always makes the decision to switch in.

- The redundant UMOD automatically switches in at the first major failure detected in the primary UMOD. (A major failure could be a malfunction in the primary UMOD's transmit or receive timing generators, a modulator failure, etc.).
- The redundant UMOD maintains a valid configuration table that contains all UMOD parameters such as interface parameters, bit rates, synthesizer frequencies, and coding types that the primary UMOD has been set for.

Manual switchover

In manual mode, the following rules apply:

- All alarms and failures are reported through the M&C to the far controller.
- The far controller must command the redundant UMOD to take over from the primary UMOD.

Returning the UMOD to normal operation after a switchover

Following a redundancy switchover, the failed primary UMOD must be replaced. Once the replacement primary UMOD has been installed and tested, the operator must initiate a Active Config command on the primary unit and then manually switch the redundant UMOD out of the circuit so the primary UMOD can begin normal operation.

Terrestrial data interface daughtercard

The terrestrial data interface daughtercard (installed on the UMOD motherboard) provides the baseband interface between UMOD and external customer DTE equipment. Either of the following data interface daughtercards can be installed:

- Data interface module (DIM)
- G.703 interface module (GIM)

The following sections describe the DIM and GIM.

DIM

The DIM daughtercard plugs into the UMOD motherboard. It functions as a data communications equipment (DCE) device and provides the electrical interface to the user's data terminal equipment (DTE) device. During transmit operations, the DIM converts RS-232, RS-422/449, or V.35 signals from the user's equipment into the TTL format required by the UMOD (see figure 3-24). During receive operations, the DIM converts the UMOD TTL signals to RS-232, RS-422/449, or V.35 electrical format. The DIM also supports data loopback capabilities for testing the UMOD.

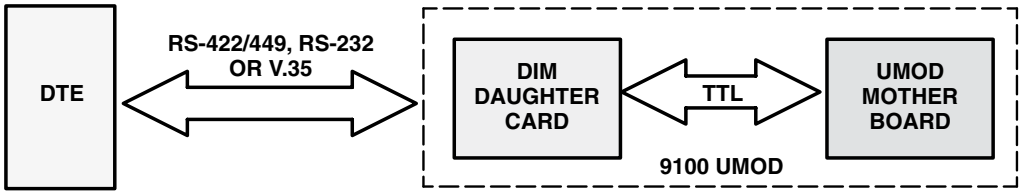

Figure 3-24 UMOD interface to user DTE device through the DIM

The DIM is controlled by the CP (located on the UMOD motherboard) through the CP interface (see figure 3-25 on page 3–42). The CP interface consists of three registers:

- Control register. This is a read/write register that the control processor uses to control DIM operation.
- Status register. This is a read-only register that the CP uses to monitor DIM status.
- Data flow register. This is a read/write register that the control processor uses to clear and set data flow control signals (CTS, DSR, and CF), and also to read back the status of DTE-generated control signals (RTS and DTR).[1]

1. Although data flow control signals are implemented in hardware, current UMOD software does not support them.

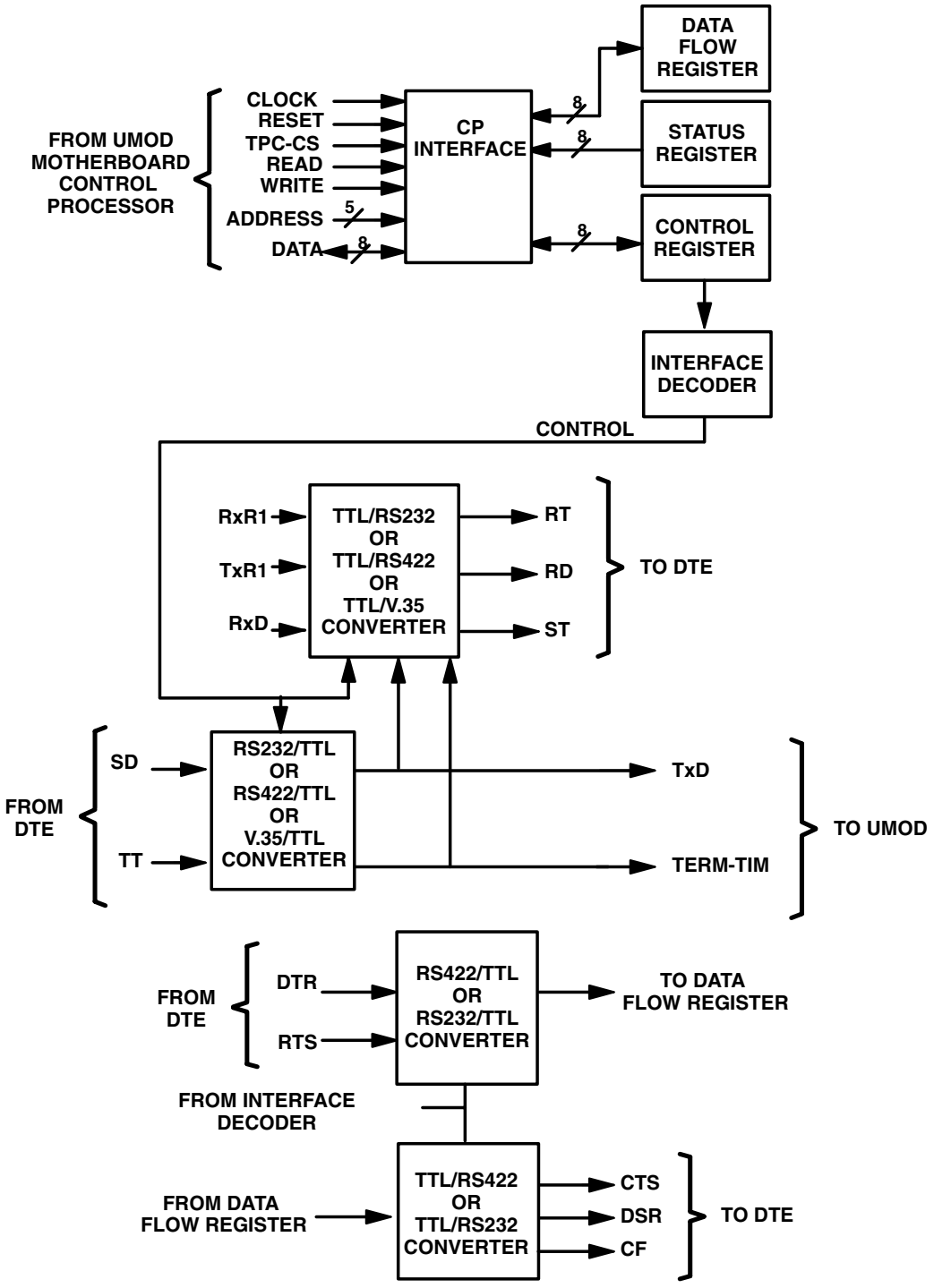

Figure 3-25 DIM block diagram

The DIM supports the baseband terrestrial interface signals by providing level translation, buffering, and termination (if required). Terrestrial interface signals include data, timing, and control signals.

Data signals

Baseband terrestrial interface data signals are as follows:

- Transmit Data (SD). SD is originated by the DTE, to be transmitted over the satellite channel by the UMOD. SD can be synchronous with either transmit clock (ST) or terminal timing clock (TT) as discussed in section “Timing Signals.”

- Receive Data (RD). This is data received by the UMOD and sent to the DTE synchronous with the RT clock. Refer to section “Timing Signals” for more information.

Timing signals

Baseband terrestrial interface clock signals are as follows:

- Transmit Clock (ST). This clock is generated at the UMOD baseband data rate and provides the DTE with transmit signal element timing information. The DTE sends the data to be transmitted (SD) to the UMOD synchronized with this clock. The transmit clock is selected as the source for transmit signal element timing, when the UMOD transmit timing generator is either referenced to the internal oscillator or to the recovered satellite clock.

  Normally the falling edge of ST indicates the center of each signal element on the SD circuit. However, the clock-to-data phase relationship is not important, as far as it meets the distortion and jitter specifications outlined in the EIA RS-334 standard. This is because the DIM provides a clock-phase-correction circuit. The phase correction circuit monitors the data transitions, and if any data transition occurs within a nominal ±12 ns of the falling edge of the transmit clock, the DIM will switch to the rising edge of the clock for retimng the transmit data.
- Terminal Timing Clock (TT). The DTE generates this clock at the UMOD terrestrial baseband data rate. This clock provides the UMOD with transmit signal element timing when the UMOD transmit timing generator is referenced to the external clock source. In this mode, the DTE sends the data to be transmitted (SD) to UMOD synchronized with this clock.

  Normally the falling edge of this clock indicates the center of each signal element on the SD signal. However, the clock

to data phase relationship is not important, as far as it meets the distortion and jitter specifications outlined in the RS-334 standard. This is because the DIM provides a clock phase correction circuitry. By default, the falling edge of the terminal timing clock (TT) is used for retiming the transmit data (SD). The phase correction circuitry monitors the data transitions, and if any data transition occurs within a nominal ±12 ns of the falling edge of the terminal timing clock, the DIM will switch to the rising edge of the clock for retiming the transmit data.

- Receive Clock (RT). The UMOD outputs the recovered clock on this circuit. RT provides the DTE with receive signal element timing information. The receive data (RT) is sent to the DTE synchronous with this clock. Normally the falling edge of the RxC occurs in the middle of the RxD data bit.

  The DIM has two modes for retiming the receive data (RD). In the *Normal* mode the data is retimed on the rising edge of the receive clock and in the *Inverted* mode the data is retimed on the falling edge. This option is software-selectable.

Control signals

The DIM Data Flow Register handles the control signals. The baseband terrestrial interface control signals are divided into DTE-generated control signals (signals coming from the user equipment) and DCE-generated control signals (signals coming from the UMOD).[2]

DTE-generated control signals. DTE-generated control signals are as follows:

- Request To Send (RTS). RTS is generated by the DTE. A transition from *OFF* to *ON* instructs the UMOD to enter the transmit mode. The CP examines the status of this signal by reading the DIM data flow register.
- DTE Ready (DTR). DTR is generated by the DTE whenever it is ready for transmitting and receiving data. The CP examines the status of this signal by reading the DIM data flow register.

DCE-generated control signals. DCE-generated control signals are as follows:

- Clear To Send (CTS). A CTS *ON* condition is an indication to the DTE that signals present on transmit data (TxD) will be transmitted over the satellite link by the UMOD. By default, until CP intervention, the DIM clears CTS into the *OFF* state.

2. The current version of UMOD software does not support control signals.

- DCE Ready (DSR). DSR is generated by the DIM data flow register and indicates that the UMOD is in data transfer mode. The *ON* condition shall not be interpreted as an indication that the satellite link has been established. By default, until CP intervention, this signal is cleared to an *OFF* condition.
- Received Line Signal Detector (CF). CF is generated by the DIM data flow register. A CF *ON* condition indicates that an RF carrier is being received and demodulated with a sufficiently low error rate for the entire receive path to remain locked to the receive signal. By default, until CP intervention, this signal is cleared to an *OFF* condition.

GIM

The GIM daughtercard plugs into the UMOD motherboard. It functions as a data communications equipment (DCE) device and provides the electrical interface to the user's data terminal equipment (DTE) device. The GIM performs appropriate HDB3, B8ZS, and B6ZS line coding or decoding, clock recovery, removes jitter from transmit data, bipolar violation alarm monitoring, loss of signal detection, and alarm indication signal (AIS) generation and detection. The GIM also supports data loopback capabilities for testing the UMOD.

Figure 3-26 shows a UMOD interfacing to a DTE device through a GIM.

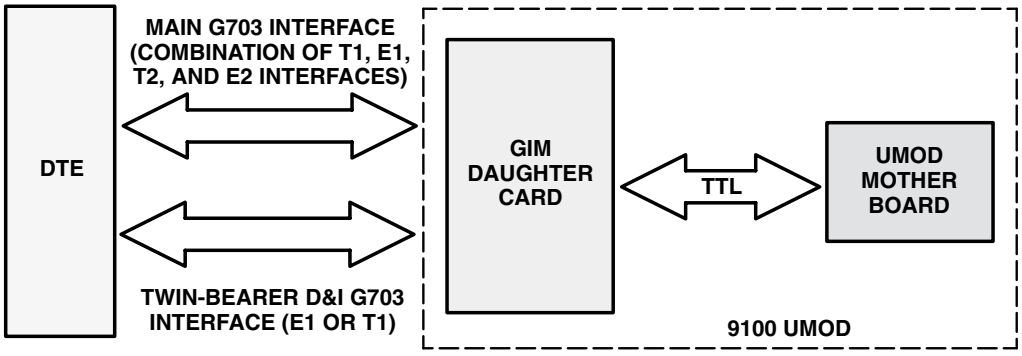

Figure 3-26 UMOD interface to DTE device through a GIM

The GIM supports two bipolar baseband interfaces: primary and twin-bearer D&1.

Primary bipolar interface

The primary bipolar interface services the main CIM data ports—RD (receive data) and SD (send data)—and is capable of operating in a mixed-rate configuration where transmit (incoming) data and receive (outgoing) data are independent and are software-selectable from the following bipolar standards: T1

(balanced), E1 (balanced or unbalanced), T2 (balanced or unbalanced), and E2 (unbalanced).

Note

The terms T1, E1, T2, and E2 describe bipolar digital data links that conform to the following electrical interfaces (as defined in CCITT G703 and T1.102):

- T1: Primary rate carrier at 1544 kbps. Also referred to as DS1.
- E1: Primary rate carrier at 2048 kbps. Also referred to as CEPT.
- T2: Secondary rate carrier at 6312 kbps. Also referred to as DS2.
- E2: Secondary rate carrier at 8448 kbps.

For example, the primary bipolar interface can receive an incoming 8448-kbps unbalanced E2 signal with HDB3 coding while generating an outgoing balanced 1544-kbps T1 signal with B8ZS coding. This flexibility, and the fact that all of the functions are under software control (with no jumpers or switches) make the GIM very versatile and easy to set up. The circuit's jitter tolerance meets CCITT G.824 and T&T TR 62411 recommendations.

E1/T1 transmit operations. In the transmit (incoming) direction, T1 or E1 data enters the GIM from the SD port of the CIM (see figure 3-27 on page 3–47). The signal is passed through a transformer, then routed to the send data (SD) E1/T1 line interface unit (LIU). The LIU extracts clock (TT) and data (TxD) from the T1 (SD-A and SD-B) or E1 (SD-A and SD-B for balanced, or SD-B for unbalanced) signals. A phase-locked loop (PLL) circuit inside the LIU locks onto the T1 or E1 signal and, using an external crystal, removes the jitter.

E1/T1 receive operations. In the receive (outgoing) direction, the receive data (RD) LIU takes clock (RxC) and data (RxD) lines from the UMOD motherboard or IFU and produces bipolar pulses of appropriate shape. The pulses are transformer-coupled and 14-dB of return loss is provided during transmission of both marks and spaces. The T1 or E1 signals are then output across the backplane to the RD port of the CIM.

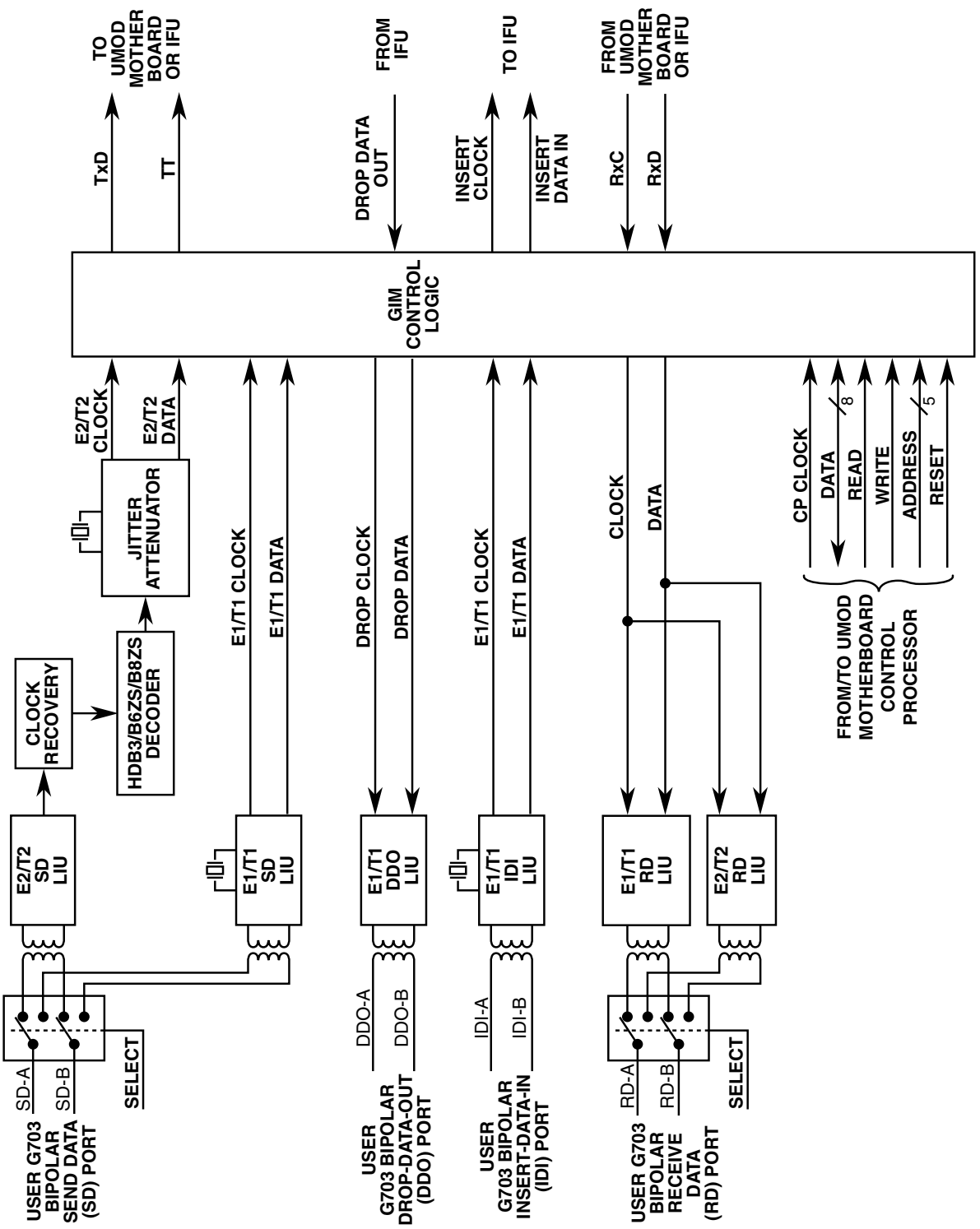

Figure 3-27 GIM block diagram

The T1/E1 LIU uses either alternate mark inversion (AMI) or B8ZS encoding for T1 signals and HDB3 encoding for E1 signals.

AMI encoding, shown in figure 3-28, is an analog representation of non-return-to-zero (NRZ) digital data. The coding rules are:

- Digital ones are converted into a series of voltage pulses of alternating polarity.
- Digital zeros are converted to no pulses (zero volts).

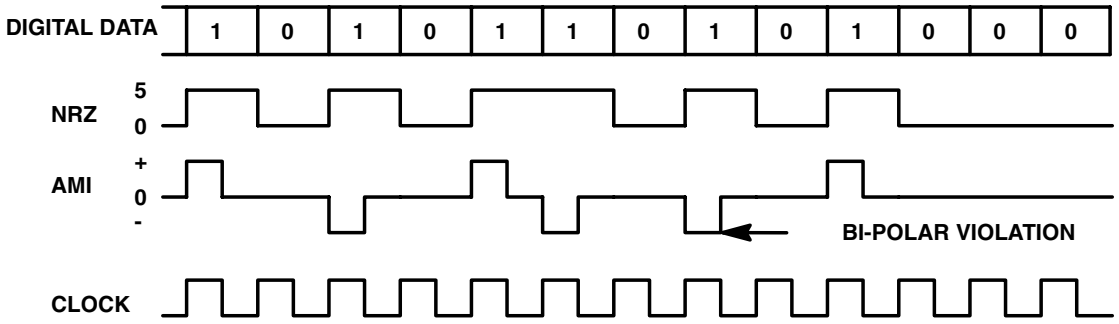

Figure 3-28 AMI encoding of digital data (NRZ)

T1 data is encoded using the analog B8ZS, a version of the AMI format. B8ZS coding does not allow more than eight successive zeros to be transmitted since zeros are represented by the lack of pulses. B8ZS substitutes a unique code that includes a combination of ones, zeros, and deliberate bipolar violations as a substitute for these zeros. This guarantees that a minimum pulse density is present for accurate clock recovery.

E1 data is encoded using the analog HDB3, a version of the AMI format. HDB3 coding does not allow more than three successive zeros to be transmitted. In the same fashion as B8ZS encoding, HDB3 substitutes a unique code as a substitute for these three zeros, guaranteeing that a minimum pulse density will be present for accurate clock recovery.

E2/T2 transmit operations. T2 (balanced or unbalanced) or E2 (unbalanced) data enters the GIM from the SD port of the CIM (see figure 3-27 on page 3–47). The signal is passed through a transformer, then routed to the SD E2/T2 LIU. The LIU extracts TT and TxD from the T2 (SD-A and SD-B for balanced, or SD-B for unbalanced) or E2 (SD-B) signals. A PLL circuit locks onto the T2 or E2 signal, the data is sampled, then clock signals and data are passed through a jitter attenuator. Appropriate decoding (HDB3, B6ZS, or B8ZS) is then performed. Clock and data signals are then routed to the IFU or UMOD motherboard for further processing.

E2/T2 receive operations. In the receive direction, the RD LIU takes RxC and RxD lines from the UMOD motherboard or IFU and produces bipolar pulses of appropriate shape. The pulses are transformer-coupled. The T2 or E2 signals are output across the backplane to the RD port of the CIM. The output signal conforms to CCITT G.703 recommendations.

Balanced T2 data is encoded using B6ZS coding, unbalanced T2 data is encoded using B8ZS line coding. (Operation using AMI coding is uncommon). B6ZS coding does not allow more than six successive zeros to be transmitted because zeros are represented by the lack of pulses. B6ZS coding substitutes a unique code that includes a combination of ones, zeros, and deliberate bipolar violations as a substitute for these zeros. This guarantees that a minimum pulse density is present for accurate clock recovery. For a description of B8ZS coding, refer to section “E1/T1 receive operations.”

Line coding for unbalanced E2 is usually HDB3 (operation using AMI coding is uncommon). For a description of HDB3, refer to section “E1/T1 receive operations.”

Twin-bearer D&I bipolar interface

Note

Twin–bearer operation in the 10–PAK chassis is limited to a balanced G.703 interface. The unbalanced G.703 does not permit twin–bearer operation.

This interface uses two separate bearers, in combination with the IFU, to support independent drop and insert multiplexers. The twin-bearer D&I bipolar interface, together with the primary bipolar interface, supports a twin-bearer drop-and-insert multiplexer. This interface uses the following CIM ports for twin-bearer operations:

- SD port and DDO (drop-data-out) port for bearer #1
- IDI (insert-data-in) port and RD port for bearer #2

Each of the twin bearers can operate independently in E1 (balanced or unbalanced) or T1 (balanced) mode. CIM ports IDI and RD provide the insert multiplexer. Ports DDO and SD provide the drop multiplexer. Normally, both drop and insert multiplexers are configured to operate at the same rate, however, because the GIM is designed to allow for a mixed-rate operation, the user can set up the drop multiplexer (SD and DDO ports) to operate in (for example) T1 mode, and the insert multiplexer (IDI and RD ports) to operate in E1 mode. For E1 operation, a mixture of balanced and unbalanced interfaces is allowed. Coding scheme selection (AMI, B8ZS, or HDB3) can be different for each port.

Drop operations. For a drop operation, a T1 or E1 bearer enters the SD port on the CIM and is routed to the SD E1/T1 LIU on the GIM. Data (TxD) and clock (TxC) are recovered and sent to the IFU and UMOD motherboard. The IFU transmit path selectively removes timeslots from the bearer, forming a lower aggregate rate to be transmitted over the satellite link. Then it either fills the selected timeslots on the bearer with idle code (01010101 for E1 or 01111111 for T1) or leaves it intact with the original data. The drop-data-out (DDO) bearer is then passed to the GIM. The DDO LIU takes this bearer and, using the TT clock signal, generates a T1 or E1 bearer. The bearer is routed across the backplane to the DDO port on the CIM, and from there to the user's DTE device (see figure 3-29).

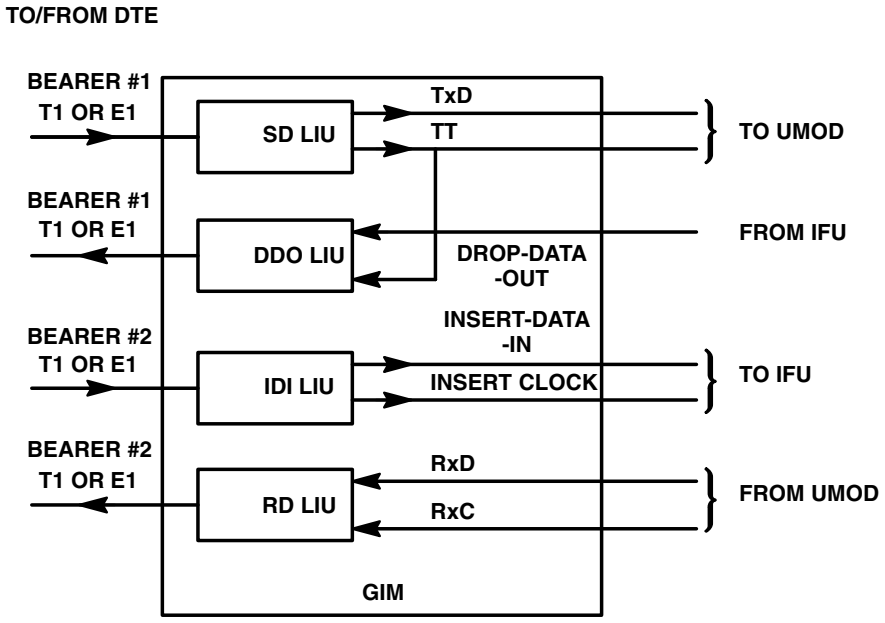

Figure 3-29 GIM twin-bearer D&I interface

Insert operations. For an insert operation, a second terrestrial T1 or E1 bearer enters the insert-data-in (IDI) port on the CIM. The data is routed to the IDI LIU on the GIM where INSERT-DATA-IN data and INSERT-CLOCK timing signals are recovered and sent to the IFU receive path through the UMOD, where the received data may be inserted into selected timeslots on the bearer. The RD LIU on the GIM takes RxD and RxC signals from the IFU and generates a T1 or E1 bearer. The bearer is routed across the backplane to the RD port on the CIM, and from there to the user's DTE device (see figure 3-29).

Internal framing unit daughtercard

The optional internal framing unit (IFU) daughtercard connects between the terrestrial data interface daughtercard (either a DIM or a GIM) and the UMOD. In open-network configurations, the IFU provides a single- or dual-bearer drop-and-insert multiplexer; and framing and buffering support for the following Intelsat and Eutelsat services:

- Intelsat Intermediate Data Rate (IDR) service
- Intelsat Business Service (IBS)
- Eutelsat Satellite Multi-Services (SMS)

The IFU buffers received data for plesiochronous operation or to negate Doppler-related timing problems caused by satellite motion; supports Engineering Service Channel (ESC) supervisory overhead; and provides backward alarm functions. Please note that IDR specifications define a SMALL IDR mode, which employs IBS–style framing. These SMALL IDR modes are invoked by selecting IBS mode for the UMOD.

IDR operation

In the IDR mode, transmit data enters the IFU through a DIM or a GIM, the ESC data is added, increasing the data rate by 96 kbps, this is then output to the UMOD motherboard for modulation (see figure 3-30).

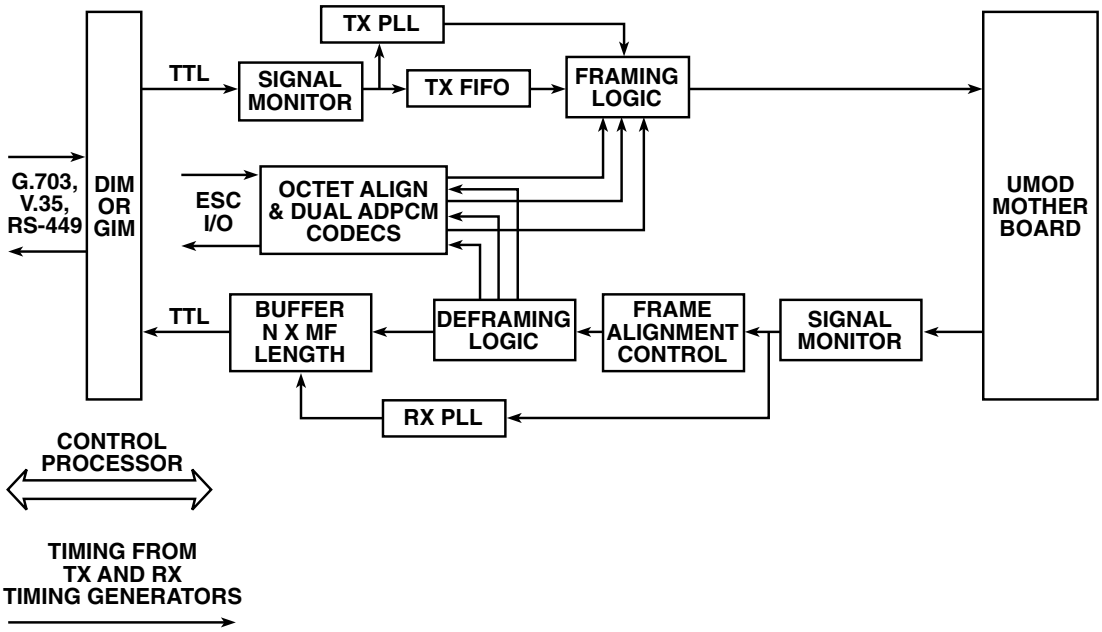

Figure 3-30 IFU IDR mode with audio ESC block diagram

In the receive direction, data enters the IFU from the UMOD motherboard. The supervisory information added at the transmit end of the link is removed, and the original data recovered. This

original data can be passed directly into the internal Doppler/plesiochronous buffer, or to the DIM or GIM. If the buffer is activated, it retimes the data so that it is synchronized to the local network clock, and provide the output to the terrestrial network through the DIM or GIM. For IDR operation, D&I multiplexers are used only when the IDR service rate is less than 1544 kbps (that is, 512 kbps, 384 kbps, and so on). **FOR ALL D&I OPERATIONS, IBS MODE MUST BE SELECTED.**

Supervisory overhead

The 96-kbps supervisory data passed over the satellite with each carrier provides several functions:

- Two 32-kbps channels—primarily for two audio ESC circuits—provide earth-station-to-earth-station links for engineering use.
- One 8-kbps data channel (with a maintained octet alignment) between stations, this provide several low-rate telegraph channels.
- Four backward alarms, for alarm signalling on multi-destination carriers.

IBS/SMS operation

In the IBS/SMS mode, transmit data enters the IFU through a DIM or a GIM, the data rate is increased by approximately 7% to accommodate supervisory information, it is then synchronously scrambled and output to the UMOD motherboard for modulation (see figure 3-31).

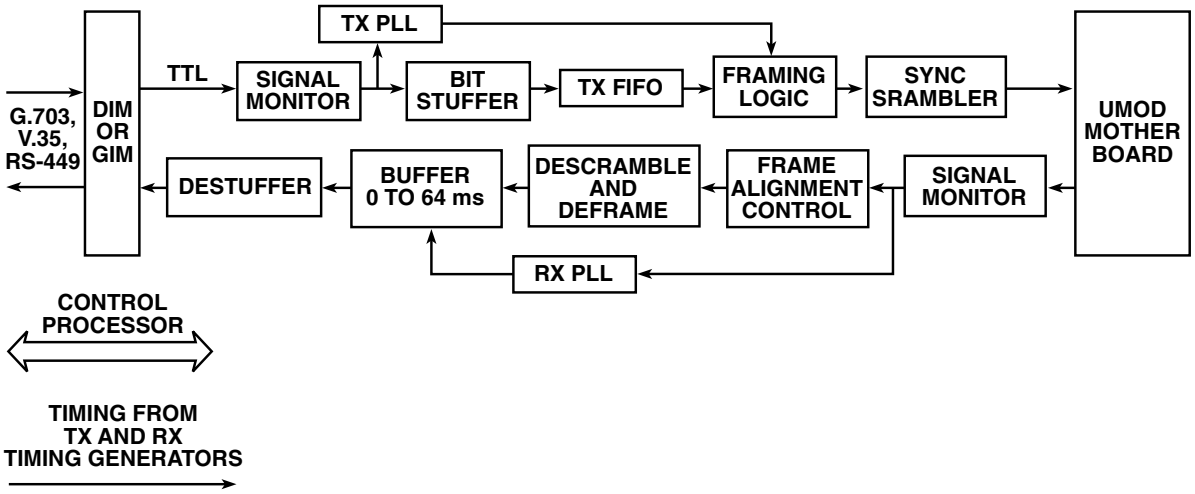

Figure 3-31 IFU IBS/SMS mode block diagram

In the receive direction, data enters the IFU from the UMOD motherboard. The signal is deframed and descrambled, the

supervisory information added at the transmit end of the link is removed, and the original data recovered. This data can either be passed directly into the internal Doppler/plesiochronous buffer, or to the GIM or DIM. If the buffer is activated, it will re–time the receive data synchronized to the local network clock, and provide the output to the terrestrial network through the DIM or GIM.

The IFU provides X.50 bit-stuffing for 48 and 56 kbps data rates. After adding satellite overhead, this results in a satellite rate of 68.26667 kbps (64 k X 16/15).

Supervisory overhead

At most multiples of 64 kbps the overhead is 6.7%, but this varies between 0% (G732-formatted 2048 kbps), 6% for 1544 kbps, 21% for 56 kbps, and 42% for 48 kbps.

The overhead added to each carrier provides several functions:

- Synchronization of the scrambler and descrambler.
- Synchronization of link encryption equipment
- A low-rate data channel, the rate of which is dependent upon the carrier rate being used
- A backward alarm facility

IFU framing modes and rates supported

The framing unit provides framing and buffering for data rates of 1.544 Mbps (T1), 2.048 Mbps (E1), 6.312 Mbps (T2), and 8.448 Mbps (E2), or buffering only for IDR data rates of 64, 192, and 384 kbps. During a transmit operation, the framing unit adds a 96-kbps ESC overhead to the regular transmit data. The overhead is used for one 8-kbps data channel, four backward alarm channels, and two 32-kbps ESC voice channels. In the receive path, the overhead data is removed and routed to the appropriate data, alarm, and ESC voice or ESC revenue channels. The original data is passed into the internal Doppler/plesiochronous buffer, and from there, after being synchronized to the local network clock, to the DIM or GIM.

Scramblers

In IBS/SMS modes, the IFU provides an IESS 309 (IBS) 2^{15} - 1 synchronous scrambler. For IDR modes, the V.35 scrambler is located on the UMOD motherboard. When optional Reed-Solomon codec is activated, only the synchronous scrambler must be used with either IBS or IDR service.

Backward alarms

Both IBS/SMS modes and IDR modes have backward alarm facilities, although the principle is the same, the practical implementation differs somewhat.

A backward alarm is a single bit of the satellite overhead, that can be sent from one station to the others. Because it is part of the overhead, sending a backward alarm does not affect the traffic. Backward alarms are sent to the far end of a satellite link to alert that there is trouble with the receive side that may be resulting from improper transmission. The UMOD M&C monitors the receive side of the link and, in the event of trouble, sends an alarm over the transmit side to the far end.

For example, stations A and B are communicating via satellite (see figure 3-32). In the event of an ongoing failure in station A (failure of the modulator output carrier for instance), there may be no indication at station A that anything is wrong. Station B will become aware of the problem when it loses frame synchronization. At this point, station A is unaware that there is a problem with the transmitted data, and station B recognizes that there is a problem receiving station A's data, but cannot determine where the fault lies.

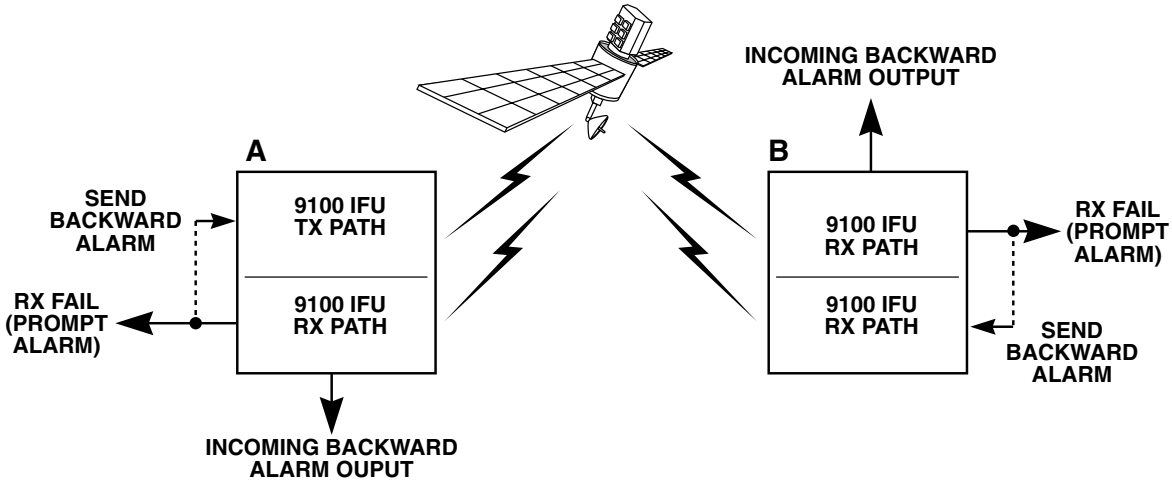

Figure 3-32 Backward alarm block diagram

Because of the lack of frame synchronization on the receive path, station B sends a backward alarm on the return data stream to station A. This does not affect the traffic in the B to A direction, but generates an alarm at station A. Station A now has a warning that there is a problem with the link from station A to B. In this situation, both stations would perform loopback tests to isolate the fault.

IBS/SMS backward alarms

IBS and SMS alarms are automatically generated by the UMOD. For example, if a receive path fails, the UMOD will automatically

generate an alarm on the outgoing transmit data.

IDR backward alarms

Backward alarms are more complicated in the IDR service because an IDR carrier can be *multi-destinational*, that is, the carrier may be received by more than one destination. All IDR carriers have four backward alarm channels.

When in IDR mode the IFU Rx prompt (SUM–RX–FAIL pin 36 of the ESC connector) may be connected to any of the four backward alarm inputs (BA1–IN through BA4–IN pins 32 through 35 of the ESC connector – see page A–7). The network operator must determine where the RX FAIL prompt alarm is connected for each site. There are four backward alarm outputs that are connected to an alarm at that site.

Single-destination carriers. These perform the same as the SMS/IBS backward alarms, but are not generated automatically. To use the IDR backward alarms, the UMOD provides an open collector copy of the receive prompt alarm on the alarms connector, this is then externally connected to the alarm input for backward alarm channel 1 (shown as the dotted line in figure 3-32 on page 3–54).

Multi-destination carriers. Figure 3-33 depicts the manner in which the four backward alarms are used.

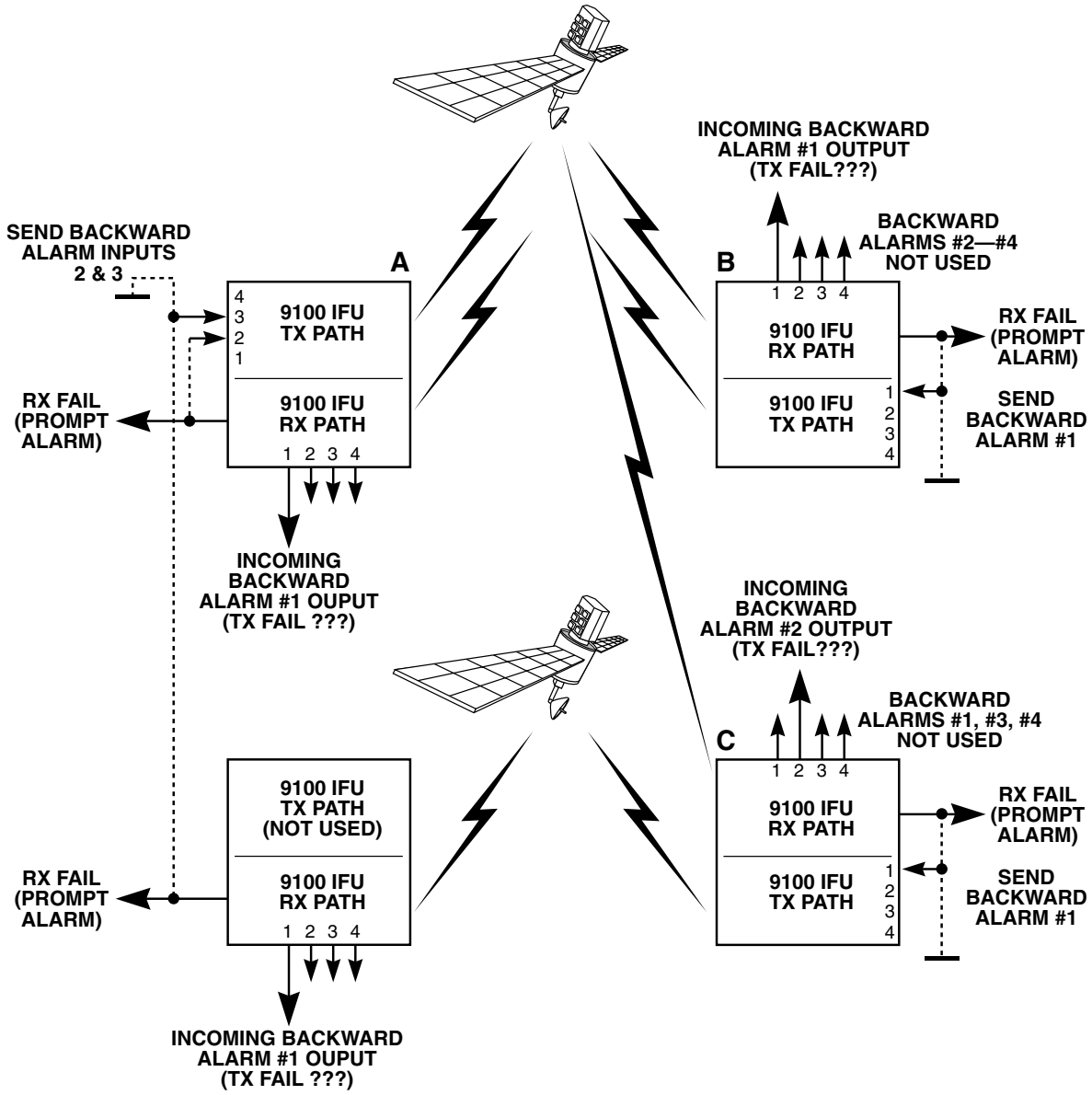

Figure 3-33 Backward alarm use with multi-destination carriers

In figure 3-33, a multi-destination carrier transmitted by station A is received by stations B and C. Both stations B and C return a single-destination carrier to station A. The backward alarms on outgoing carriers from B and C are configured the same as for a single-destination carrier, that is, the receive prompt alarm activates backward alarm channel number 1.

At station A, however, there are two receive channels, but only a single transmit channel. Here the receive prompt alarms from the two receive sections activate two separate outgoing backward alarms. The carrier from station B activates backward alarm 2, and the carrier from station C activates backward alarm 3.

The important points to understand are:

- Both B and C receive two possible incoming alarms, channel two for station B and channel three for station C. Both B and C implement only the alarm channel for their particular station, as for example the alarm #2 from station A, which indicates a possible transmit failure of station B, is of no use at station C. Hence in the diagram above, only one incoming alarm is used at each of B and C.
- Station A receives two separate incoming alarms:
  - The alarm from station B indicates either station A transmit failure, or station B receive failure.
  - The alarm from station C indicates either station A transmit failure, or station C receive failure.

This partially removes the backward alarm ambiguity, where it is not known if the alarm is a result of the near transmit end simultaneously, or the far receive end. Now if station A transmit fails, both B and C will generate an alarm, however if B or C receive fail, only one incoming alarm will be generated.

Buffer

The UMOD Doppler/plesiochronous buffer accommodates all IDR/IBS data rates and clock configurations. Buffer depth is variable and is dependent on the data rate and clock configuration of the UMOD.

The Doppler buffer is a FIFO comprising a write pointer, a read pointer, a depth pointer register, control logic, and a 64 K x 8-bit SRAM used as the data storage array. The buffer operates as a circular queue where each pointer rolls over upon reaching maximum count and then reloads with the value programmed into the depth register. The CP first initializes the buffer by programming the depth pointer register and then programming the write pointer halfway between the depth value and maximum count. The read pointer is always initialized to the value in the depth register by the control logic. During operation the control logic monitors the read and write pointers for overflow/underflow violations. When a violation occurs, the control logic reinitializes the pointers to same state as when initialized by the CP. Overlow/underflow status is made available to the CP and is cleared when read.

Drop and Insert

The drop-and-insert (D&I) feature enables the UMOD to extract (drop) timeslots from an incoming T1, E1, or CEPT bearer, transmit those outgoing timeslots at a reduced aggregate rate, and place (insert) received incoming timeslots onto preselected timeslots in the outgoing bearer. The UMOD supports three types of D&I operations: single-bearer, twin-bearer, and cascading (see figure 3-34).

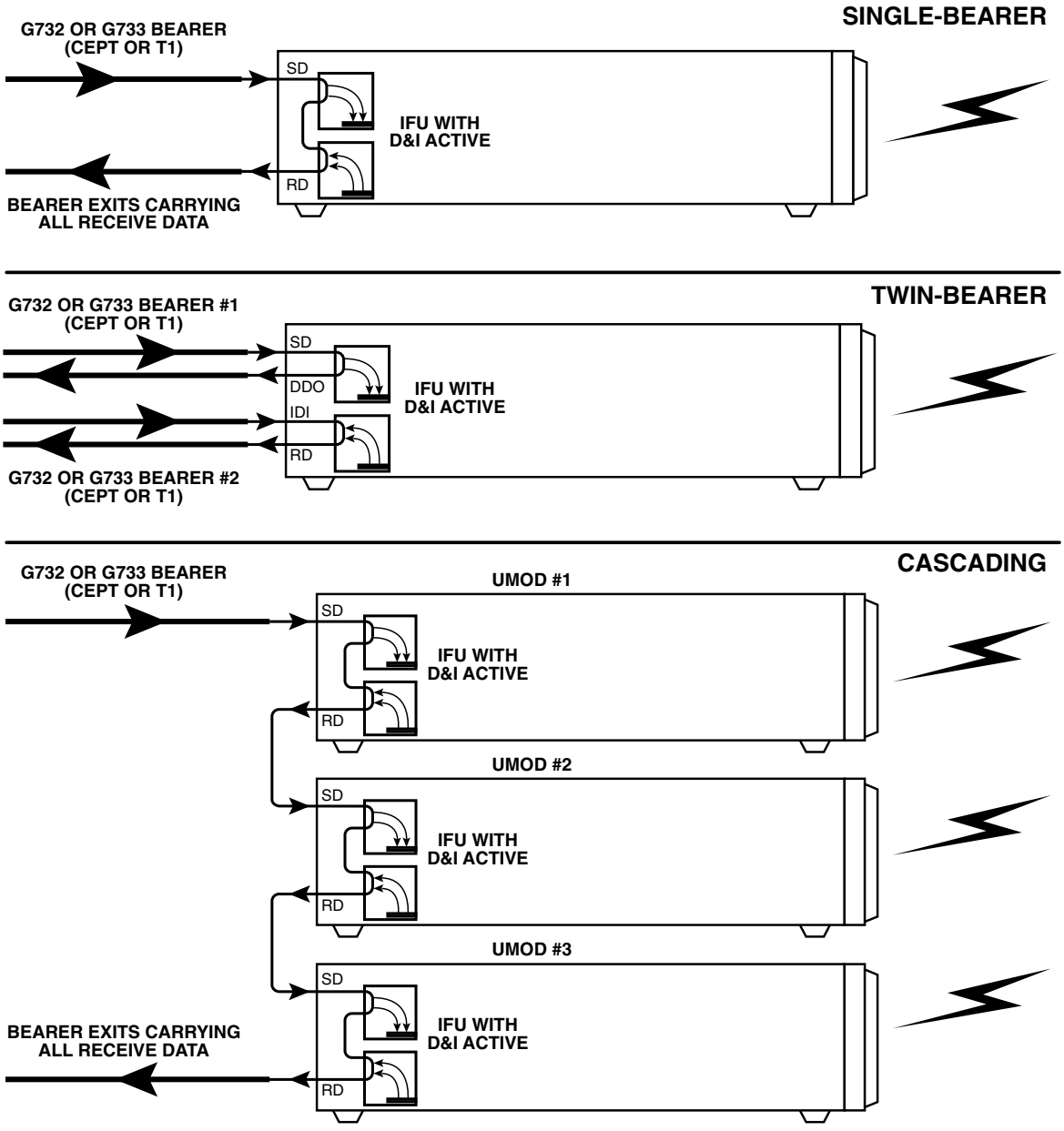

Figure 3-34 Drop-and-insert configurations

Single-bearer D&I operation

In the single-bearer configuration, the CIM ports can be configured as follows (see figure 3-35):

- The transmit (drop data) cable is connected to port SD (send data), and the receive (insert data) cable is connected to port RD (receive data).

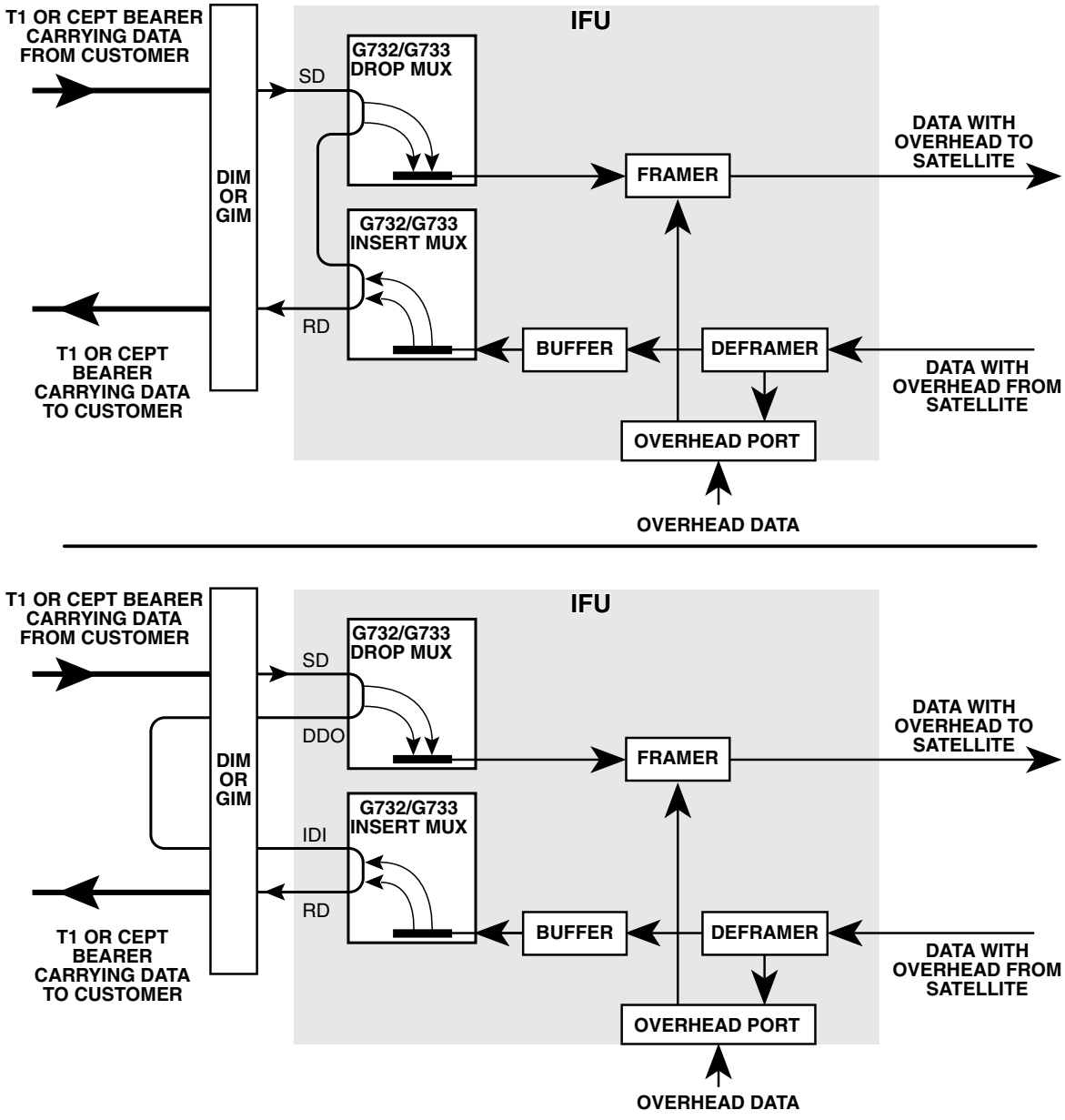

Figure 3-35 Single-bearer D&I configurations

- The transmit (drop data) cable is connected to port SD (send data). A short cable connects to the DDO (drop-data-out) and IDI (insert-data-in) ports. The receive (insert data) cable is connected to port RD (receive data).

The IFU D&I feature consists of a G732/G733 drop multiplexer (MUX) and a G732/G733 insert multiplexer (see figure 3-35 on page 3–59).

In the transmit direction, a T1 or CEPT bearer passes into the IFU drop multiplexer. The drop mux drops preselected frames from the bearer, forming a lower aggregate rate (which is M x 64 kbps). Then the multiplexer either fills the selected timeslots on the bearer with idle code (01010101 for E1 or 01111111 for T1) or leaves the timeslots intact with the original data. The dropped frames are routed to the framer, then output to the UMOD motherboard. Meanwhile, the T1 or CEPT bearer is passed to the receive path, where the insert mux inserts incoming frames into preselected timeslots on the bearer. Timeslots not selected for drop or insert operations are passed unaltered through the IFU.

For T1-D4/T-ESF bearer, any timeslots from 1 through 24 can be selected. For G732 (E1 or CEPT) any timeslots from 1 through 31 may be selected. Timeslot selection is independent for transmit (drop) and receive (insert). In addition to M x 64 kbps, the D&I multiplexers can drop-and-insert an entire T1 bearer on a 2048-kbps G732 bearer. Doing so uses the first available 24 + 1/8 timeslots (including timeslot 16 of the G732 bearer).

Twin-bearer D&I operation

Note

Twin–bearer operation in the 10–PAK chassis is limited to a balanced G.703 interface. The unbalanced G.703 does not permit twin–bearer operation.

The UMOD can be configured to D&I two bipolar, balanced bearers. When a twin-bearer configuration is used, the IFU is configured as shown in figure 3-36, with the drop multiplexer completely independent from the insert multiplexer. In this configuration, the CIM ports are configured as follows:

- For bearer #1, ports SD (send data) and DDO (dropped-data-out) are used for the drop operation.
- For bearer #2, ports IDI (insert-data-in) and RD (receive data) are used for the insert operation.

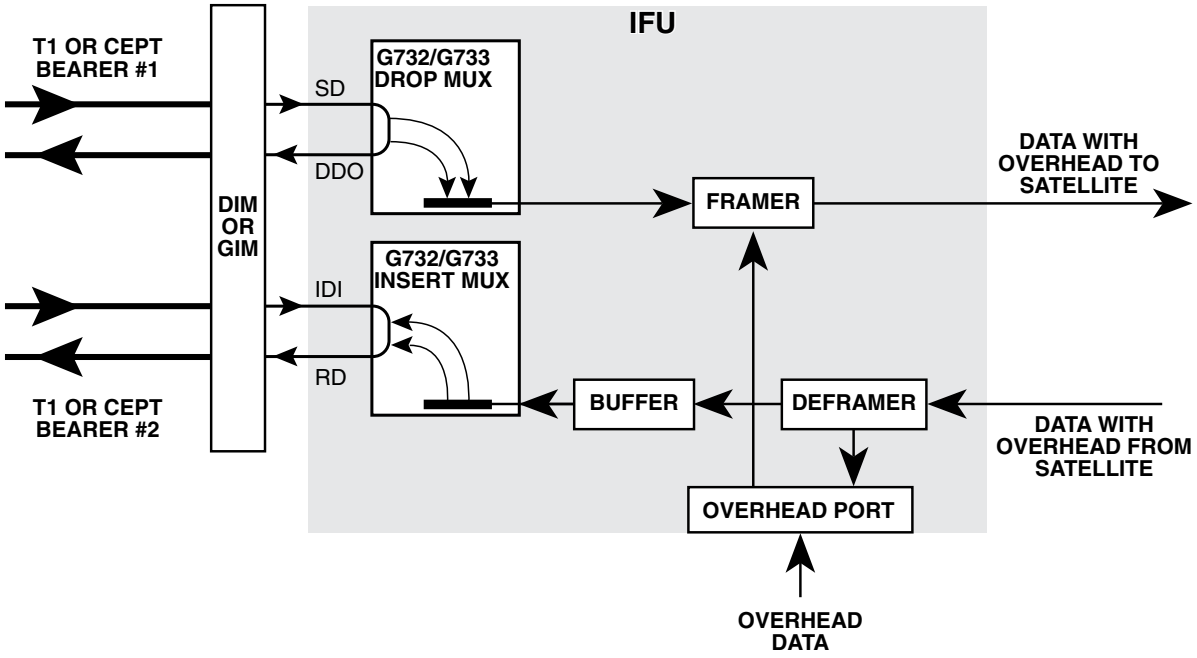

Figure 3-36 Twin-bearer D&I operation

Cascading D&I operation

The IFU D&I feature enables multiple UMOD chassis to be cascaded, eliminating T1 or CEPT multiplexer equipment in many instances.

As shown in figure 3-37, a single bearer enters the station carrying several low-rate channels. Each IFU drops the appropriate data from the bearer and transmits it over satellite, the received data is inserted into the same bearer.

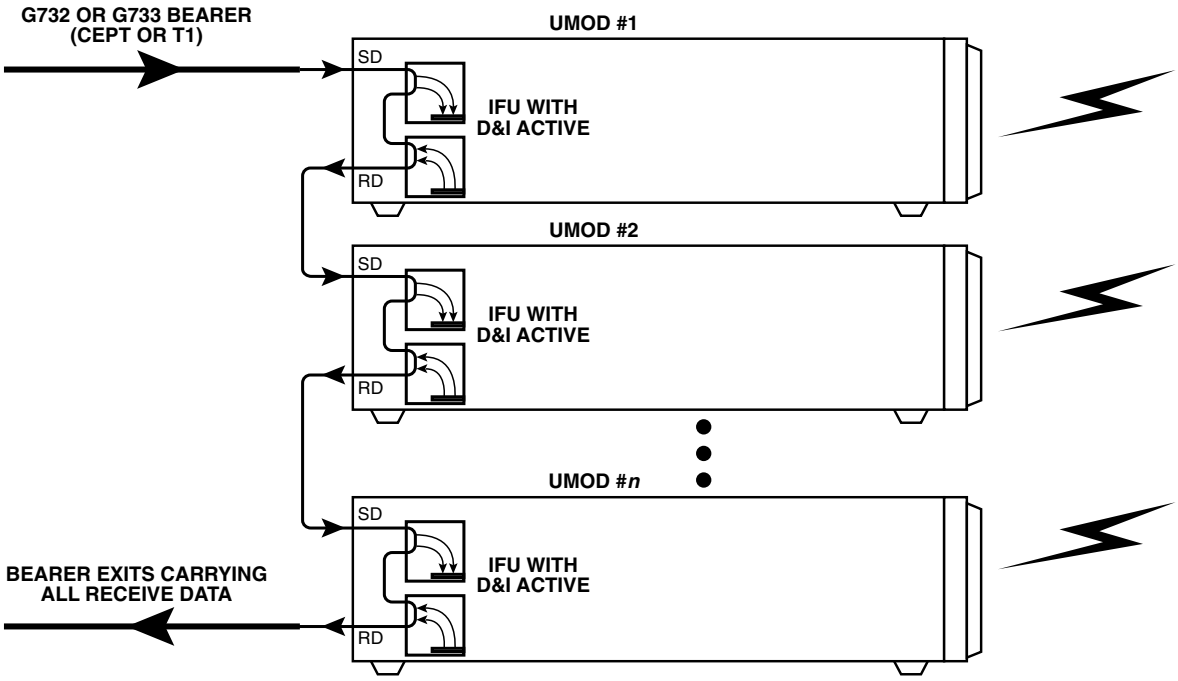

Figure 3-37 Cascading D&I operation

D&I using a composite carrier

Each IFU can be set to D&I any combination of timeslots, therefore several users' data can be combined onto a single composite carrier. The IBS/SMS satellite overhead maintains each timeslot's identity as it is routed across the satellite link, so that several data channels may be dropped from a bearer, transmitted via satellite at an aggregate rate, and then recovered separately at the receive side of the link. The receiving IFU inserts the receive timeslots anywhere in the receive bearer following the original sequence (that is, the first dropped timeslot will be the first timeslot inserted).

As an example showing the advantages of using a composite carrier, let's say several users' data channels are going to be

combined onto the same carrier. If the second and third carriers are 64 kbps and 128 kbps and are intended for the same destination, one entire modem/framing unit will be saved, by carrying both users' data in a single 192-kbps carrier.

3.8

Loopback tests and bit error rate tester functions

The UMOD provides loopback tests and a built-in bit error rate tester (BERT) as simple methods for verifying satellite link performance and UMOD/RF equipment operation. Loopback tests perform near or over-the-air link tests. The source of data may be either external (normal user traffic through the terrestrial data interface daughtercard) or the BERT.

To perform a loopback test, the user first determines how much of the communications link should be tested. The options are as follows:

- Test just the components inside the near UMOD
- Test the UMOD, RF equipment, and the satellite
- Perform a full loopback where both the near and far UMODs are tested

The user's DTE device transmits data through the portion of the communications link being tested (the BERT can also be used to transmit test data), which then loops the data back to the DTE device (or the BERT) as received data. The user then compares the received data against the transmitted data to check for errors.

Loopback tests description

Loopbacks tests enables the user to troubleshoot most satellite and equipment malfunctions without requiring external test instruments. The UMOD can perform the following loopback tests:

- IF loopback (see figure 3-38 on page 3–63). Connects the transmit IF signal to the receive IF signal. Again, the transmit and receive configuration parameters must match.

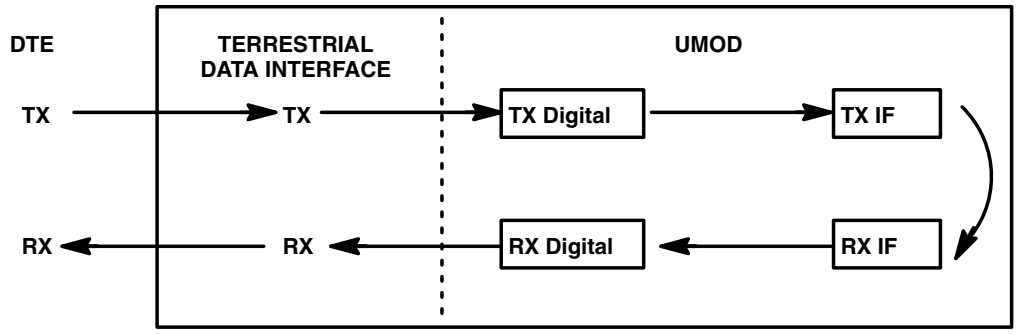

Figure 3-38 IF loopback

- Near loopback. As shown in figure 3-39, a near loopback receives user data at the near UMOD, loops the data through the DIM or GIM, and transmits it back to the user device. This loopback verifies that user equipment, connecting cables, and UMOD terrestrial data interface circuits are functional.

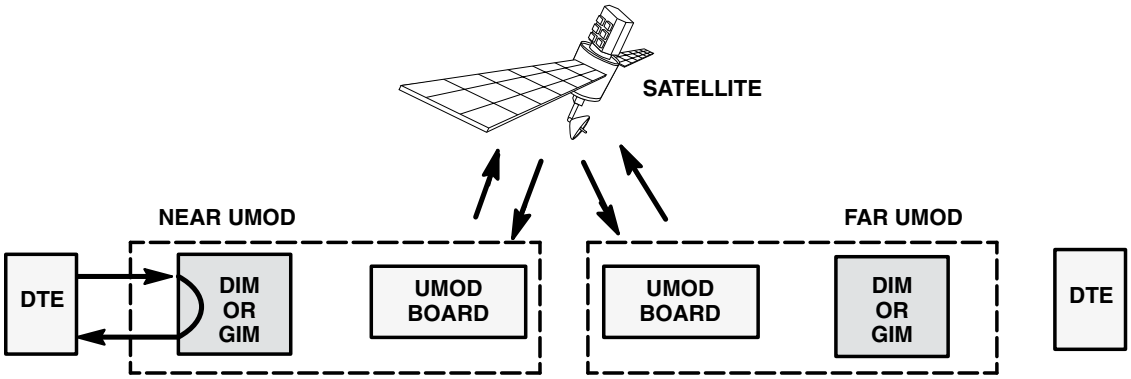

Figure 3-39 System-level view of the near loopback

- Far loopback. A shown in figure 3-40, a far loopback is a complete test of the near UMOD and most of the far system excepting the far DTE device. The far loopback tests the following equipment:
  - Near DTE device and connecting cables
  - Near UMOD, radio frequency terminal (RFT), and antenna subsystem
  - Satellite transponder
  - Far UMOD, RFT, and antenna subsystem

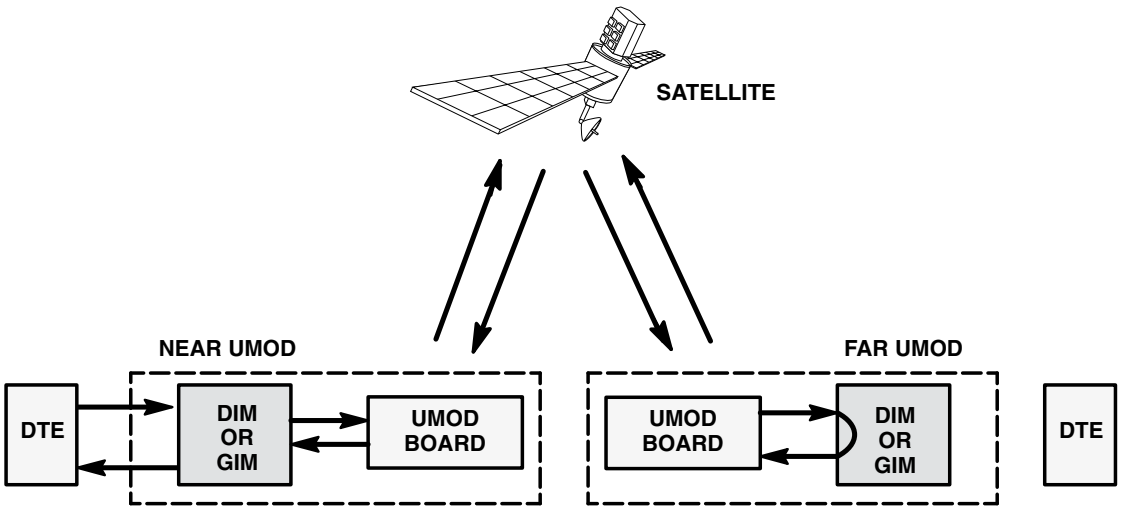

Figure 3-40 System-level view of the far loopback

- Simultaneous loopback (see figure 3-41). This loopback configures one of the UMODs to perform a near and far loopback test. If the UMOD at the far end of the link is set to perform a far loopback, the combined tests will verify functioning of all components in the communications link.

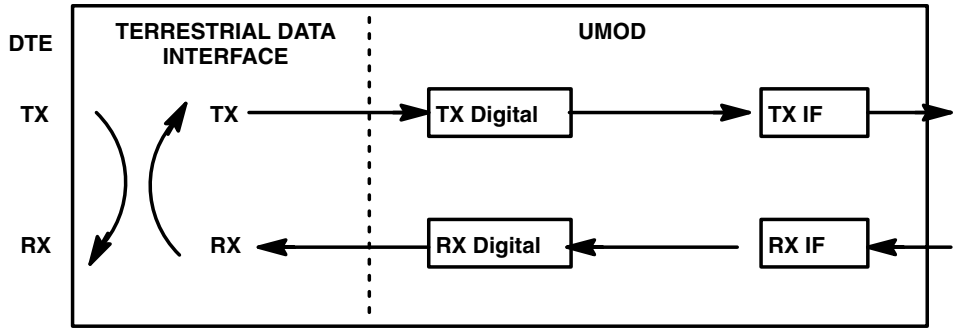

Figure 3-41 Simultaneous loopback

BERT description

The BERT function, in combination with the loopback tests, enables the user to test various UMOD components. The BERT function consists of an independent transmit pattern generator and a receive error analyzer. Transmit BERT pattern generator parameters are as follows:

- Industry-standard 511-bit m-length pseudo-random sequence
- 8-bit user-entered repetitive pattern
- All l's
- All 0's
- 1010... repetitive
- 6-bit user-entered repetitive pattern
- Insert a single error

The BERT error analyzer works with the pattern generator at the transmit end. Methods for evaluating error patterns are as follows:

- Bit error rate
- Average bit error rate
- Block error rate
- Sync loss

The BERT receive analyzer consists of a 2^{28} - 1 bit counter, a 2^{28} - 1 bit error counter, a 2^{17} - 1 block counter, and a 2^{17} - 1 block error counter.

BERT loopback connections

The BERT performs the following loopback connections:

- Normal loopback (see figure 3-42). This test connects the loopback transmit and receive to the normal satellite data.

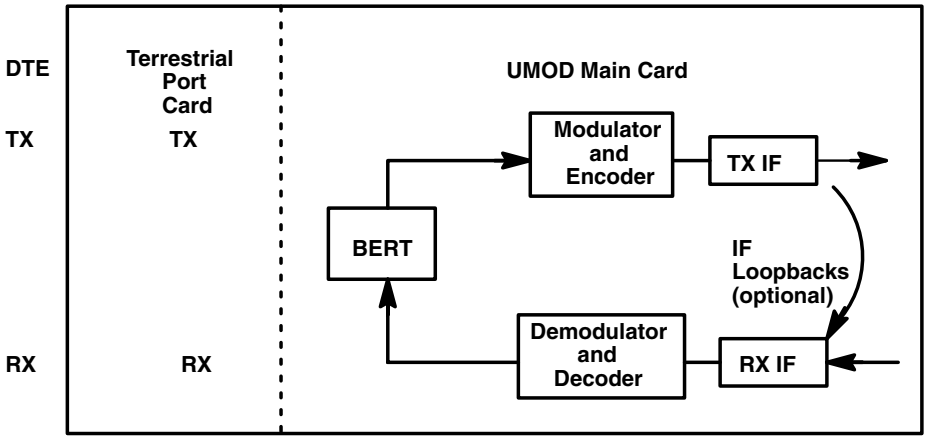

Figure 3-42 Normal BERT loopback connection

- Terrestrial data interface (see figure 3-43). This loopback connects the BERT to the terrestrial data interface (either a DIM or GIM). This option can be combined with either the general Near or Far loopback commands.

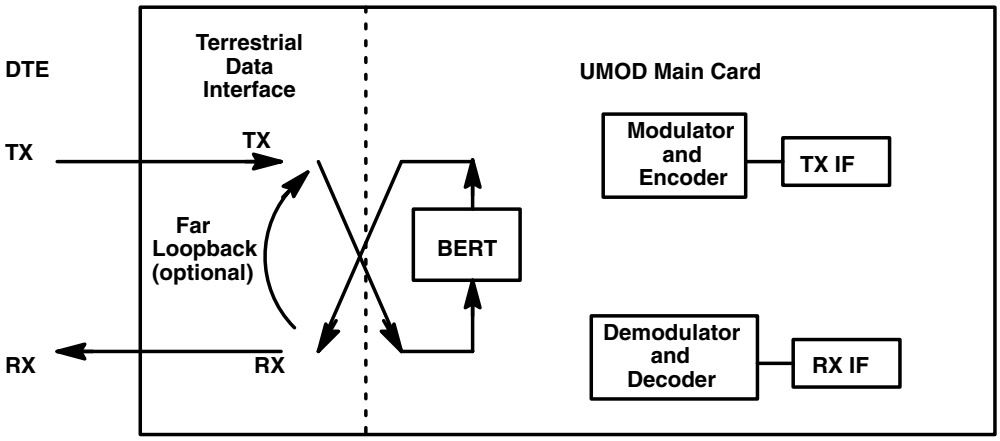

Figure 3-43 Terrestrial data interface BERT loopback connection

- IFU loopback (see figure 3-44). This loopback connects the transmit output from the BERT to the input of the internal framing unit (IFU). The receive data from the IFU is connected to the BERT. The transmit and receive configuration parameters must be the same (that is, if the UMOD is configured for QPSK transmit modulation and BPSK receive modulation, the modulation for both transmit and receive must be set for QPSK or BPSK before running the loopback).

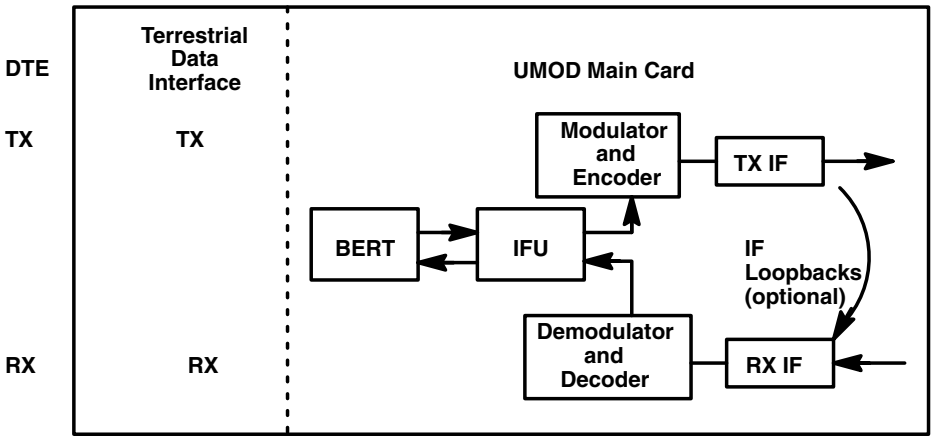

Figure 3-44 Loopback connections with BERT and IFU enabled

3.9

UMOD timing configurations

UMOD system timing is one of the most critical areas of operation. Timing problems can result in increased BER, synchronization loss, and other satellite communications problems. The UMOD supports synchronous data communications, and requires stable and synchronous clock signals and data to ensure reliable link operations.

The UMOD has a variety of clocking modes. This section explains each mode and clarifies the proper configuration for each mode when the UMOD is configured with the DIM. Please note that, for completeness, software versions are referenced. The software version is available by requesting ver from the Terminal Interface or Detailed Status screen from the UMOD M&C.

The first two subsections, Transmit and Receive, provide explanations of the timing modes and their clock source options. figure 3-45 on page 3–69 provides a block diagram of the transmit and receive functions.

The remaining sections explain how to connect the UMOD for proper operation in *looped–timed* systems and in

independent–timed systems using either plesiochronous or non–plesiochronous configurations.

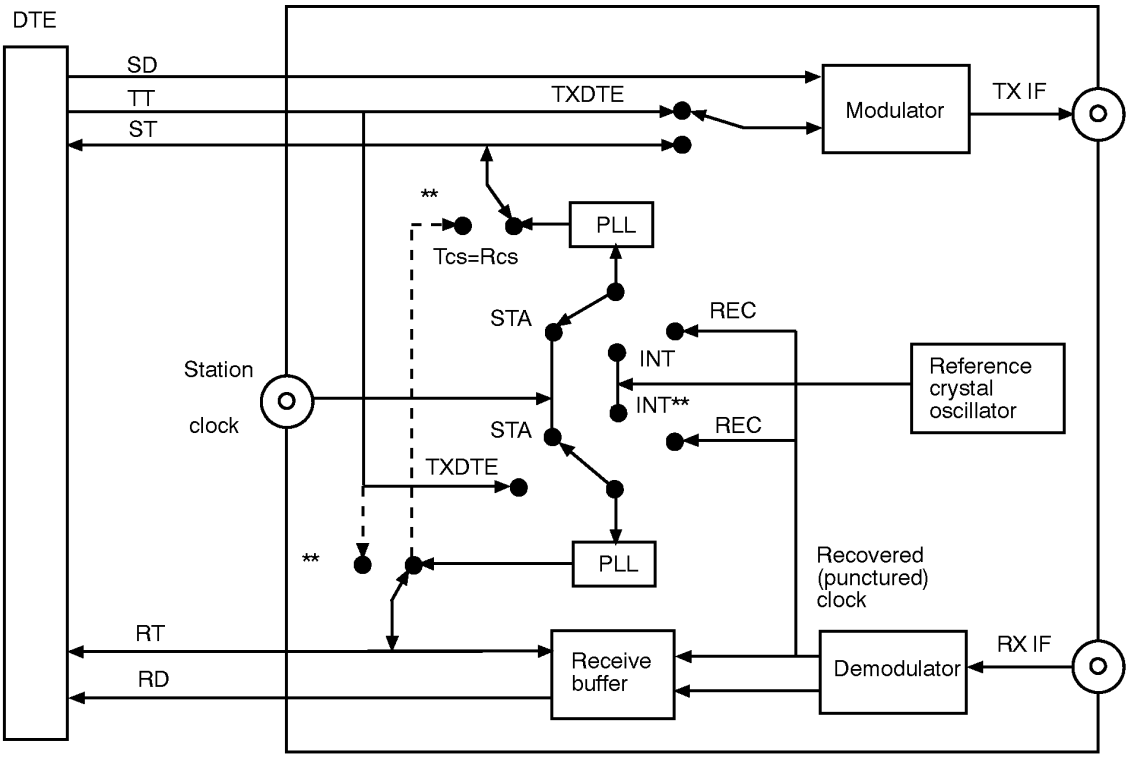

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Figure 3-45 UMOD transmit and receive timing functional block diagram

** Indicates availability in UMOD software release 3.03 and above.

3.10

Transmit timing modes

For the modulator there are four transmit clock source options (TCS) or modes: internal (INT), TXDTE external terminal timing (TT), external station clock input (STA), and recovered from Demod (REC).

Internal transmit clock selection

The selection of INT TCS uses the UMOD;s internal TCXO crystal oscillator reference to generate the send timing (ST) clock. The transmitted symbol rate is locked to this ST clock. The TT clock input is ignored for this mode.

TXDTE transmit clock selection

This selection of TXDTE TCS uses the external TT clock input from the data terminal equipment (DTE). The transmitted symbol rate is locked to this TT clock. The ST clock is inhibited for this

mode. Use this mode only when the TT clock's stability is within the UMOD specification (± 100ppm).

Clock fault operation

If this clock input completely disappears, the UMOD will generate a Tx ext clock fail condition and will continue to transmit using the internal clock as reference. When the clock reappears, normal operation will resume.

When this clock input becomes noisy or is at the wrong frequency (outside 250 ppm of nominal) for UMOD software release 2.01 or lower, the UMOD will stop transmitting and will set a fatal alarm F10. The UMOD will not restart unless the **GO** or **GOTX** command is issued via the terminal interface port, or ACTIVATE or ACTIVATE TX is entered from the M&C Configuration screen.

For UMOD software release 3.03 or above, when this clock input becomes noisy or is at the wrong frequency (outside 250 ppm of nominal), the UMOD will stop transmitting, send out a warning, and when the clock returns within specification, the carrier will automatically return.

Station transmit clock selection

Selecting STA TCS uses the external Station BNC clock input to generate the ST clock. The station clock can be at any pre–defined frequency from 1 to 10 MHz and is independent of data rate. The station clock and the generated ST clock are phase locked but are not phase coherent. The STA and ST clocks do not have to be at the same frequency. The transmitted symbol rate is locked to this ST clock. The TT clock input is ignored for this mode.

Clock fault operation

If this clock input completely disappears, the UMOD will generate a Tx ext clock fail condition and will continue to transmit using the internal clock as reference. When the clock reappears, normal operation will resume.

When this clock input becomes noisy or is at the wrong frequency (outside 250 ppm of nominal) for UMOD software release 2.01 or lower, the UMOD will stop transmitting and will set a fatal alarm F10. The UMOD will not restart unless the **GO** or **GOTX** command is issued via the terminal interface port, or ACTIVATE or ACTIVATE TX is entered from the M&C Configuration screen.

For UMOD software release 3.03 or above, when this clock input becomes noisy or is at the wrong frequency (outside 250 ppm of nominal), the UMOD will stop transmitting, send out a warning, and when the clock returns within specification, the carrier will automatically return.

Recovered transmit clock selection

Selecting REC TCS uses the punctured receive Demod clock to generate the ST clock. The TT clock input is ignored for this mode. The transmitted symbol rate is locked to this ST clock.

When the RT and ST clocks are the same frequency but are not phase coherent, they can drift ± 12–bit periods.

If the Demod is not locked the UMOD will generate a Tx ext clock fail condition, the ST clock will use the internal clock as a reference. When the Demod becomes locked, the ST clock will use the receive Demod clock as the reference.

3.11

Receive timing modes

There are three receive clock selections (RCS) or modes for the demodulator: recovered from Demos (REC), TXDTE external terminal timing (TT), and external station clock input (STA). For software release 3.03 and above there is a fourth mode: internal (INT).

Recovered receive clock selection

Selecting REC RCS mode uses the recovered Demod clock to generate the RT clock.

Clock fault operation

If the Demod is not locked the UMOD will generate a Rx Acq: SRCH condition, and the RT clock will use the internal clock as a reference. When the Demos becomes locked, the RT clock will use the receive Demod clock as the reference.

TXDTE receive clock selection

The TXDTE receive clock selection of (RCS) uses the external terminal timing (TT) clock input from the DTE to generate the RT clock.

Clock fault operation

While RCS=TXTDE if the Tx Clk Source TCS=INT, STA or REC, there will not be an Rx Clk Failure condition because the Rx PLL always generates the clock. When RCS and TCS=TXDTE and the clock input completely disappears, the UMOD generates an Rx Clk Fail condition and the RT clock will default to internal. When the clock reappears, normal operation resumes.

For UMOD software release 2.01 or lower, when RCS and TCS=TXDTE and this clock input becomes noisy or is at the wrong frequency (outside 250 ppm of nominal) the UMOD sets a fatal alarm F12 and the receive side of the UMOD is deactivated. The UMOD will not restart unless the **GO** or **GOTX** command is issued via the terminal interface port, or ACTIVATE or ACTIVATE TX is entered from the M&C Configuration screen.

For UMOD software release 3.03 or above, when this clock input becomes noisy or is at the wrong frequency (outside 250 ppm of nominal), the UMOD will default to internal clock. When the clock reappears, normal operation will resume.

Station receive clock selection

Selecting the STA RCS mode uses the external station BNC clock input to generate the RT clock. The station STA clock and the

generated RT clock are phase locked but are not phase coherent. The STA and RT clocks do not have to be at the same frequency.

Note

While in this mode, the PLL will reference the internal oscillator if there is no station clock input.

Clock fault operation

If this clock input completely disappears, the UMOD will generate an external clock failure condition, and the RT clock will default to internal clock. When the clock reappears, normal operation will resume.

For UMOD software release 2.01 or lower, when this clock input becomes noisy or is at the wrong frequency (outside 250 ppm of nominal), UMOD will set Fatal alarm F12 and the receive side of the UMOD is deactivated. The UMOD receive side will not restart until the M&C receives a **GO** or **GORX** command.

For UMOD software release 3.03 or above, when this clock input becomes noisy or is at the wring frequency (outside 250 ppm of nominal), UMOD defaults to internal clock. When the clock reappears, normal operation will resume.

Internal receive clock selection

Selecting the INT RCS mode uses the UMOD's internal reference TCXO crystal oscillator reference to generate the RT clock.

Note

This internal mode for an RCS selection is only available for software release 3.03 and higher.

3.12

Looped–timed systems

In a loop-timed system, the far (or slave) UMOD clocks its transmit data (SD) with the recovered receive timing signal (RT) taken from the signal transmitted by the near (or master) UMOD. The slave UMOD must be able to withstand variations in the transmitted clock caused by Doppler shift, as well as other propagation delays that occur during communications over satellite links, otherwise synchronization with the received data will be lost.

The UMOD's Doppler/plesiochronous buffer allows newly-received data to be clocked with the RxC signal recovered from the receive data. Once loaded into the buffer, the data is held until it can be released in synchronization with the UMOD's or DTE device's timing source. Without the buffer, there would be no way to allow for short-term fluctuations between the receive and transmit clock.

This section describes loop–timed systems with phase coherent and limited phase coherent DTE for different software versions. Software versions are grouped as 2.01 and lower, and 3.03 and higher.

Looped–timed systems phase coherent DTE

For software version 2.01 and lower. The looped–timed systems configurations for software versions 2.01 and lower are illustrated in figures 3-46 and 3-47and assume the following:

- The DTE data rates are all the same
- The DTE requires a slaved phase relationship where no phase wander is allowed
- If station clock is used, input must be within ±100 ppm
- For the *near* or *master* end, set Buffer ON, TCS must be set to TXDTE, and RCS must be set to Station (with or without station clock)
- For the *far* or *slave* end, set Buffer OFF, RCS must be set to Recovered, and TCS must be set to TXDTE.

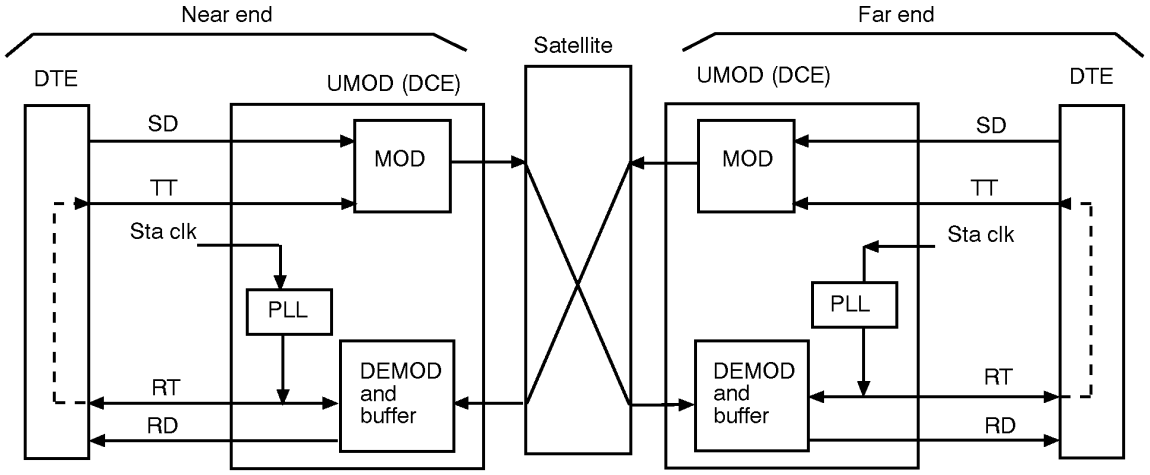

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Figure 3-46 Looped–timed system, phase coherency with station clock (SW 2.01)

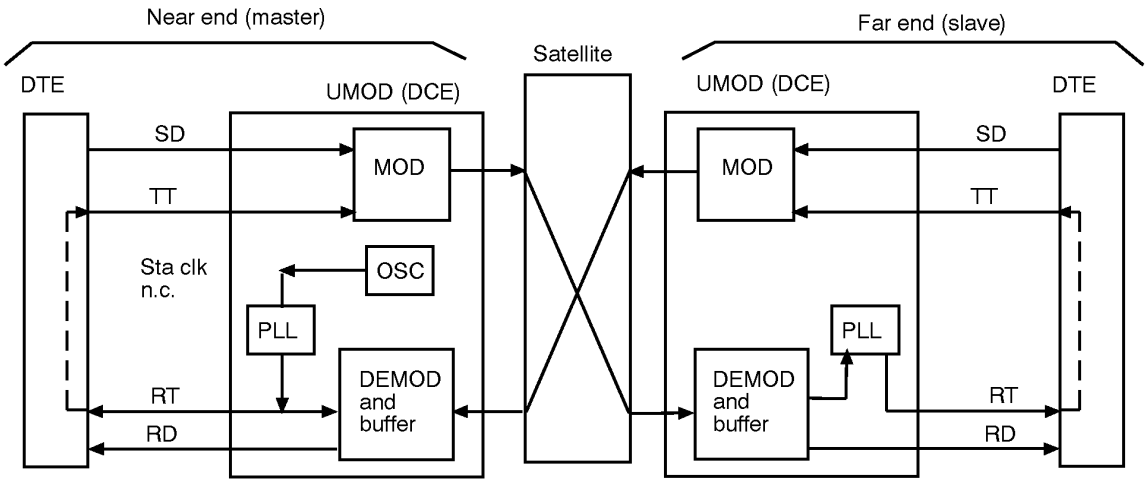

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Figure 3-47 Looped–timed system, phase coherency without external clock (SW 2.01)

Looped–timed sys. limited coherent DTE

For software version 2.01 and lower. The examples shown in figures 3-48, 3-49, and 3-50 illustrate looped–timed systems with limited phase coherency, and assume the following:

- The DTE data rates do not have to be the same
- The DTE will allow phase wander up to ± 3 bits if data rates are the same
- If the DTE clock is used, it must be within ± 100 ppm
- If station clock is used, input must be within ± 100 ppm
- For the *near* or *master* end, set Buffer ON and:
  - If DTE clock is used, set TCS to TXDTE, and RCS to TXDTE (see figure 3-48)
  - If station clock is used, set TCS to Station, and RCS to Station (see figure 3-49)
  - If internal clock is used, set TCS to Internal, and RCS to Station with no station clock input (see figure 3-50)
- For the *far* or *slave* end, set Buffer OFF (RCS must be set to Recovered, and TCS must be set to TXDTE).

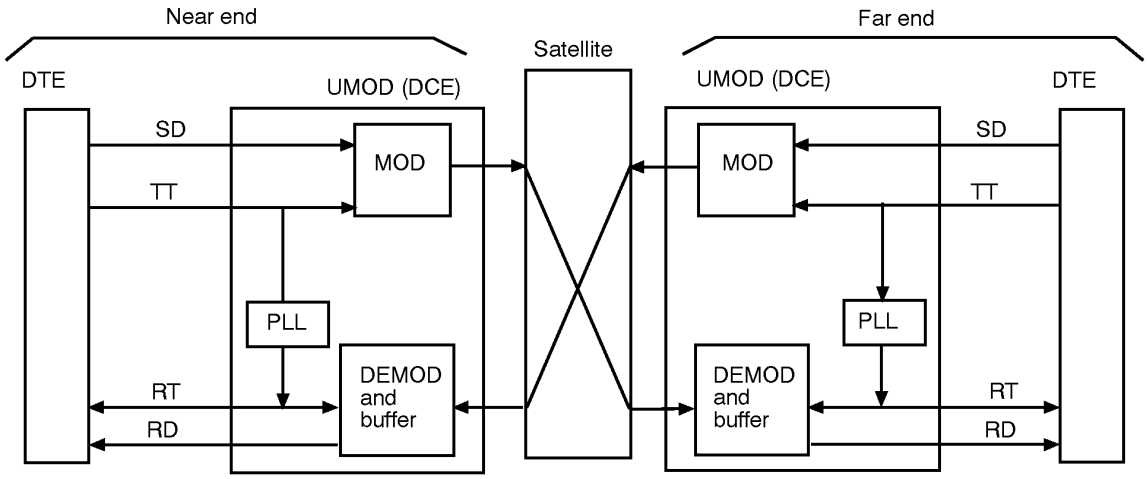

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Figure 3-48 Looped–timed, limited phase coherency, DTE clock reference (SW 2.01)

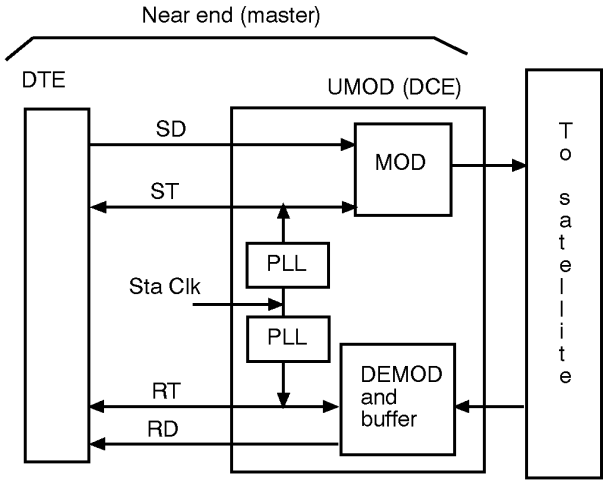

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Figure 3-49 Looped–timed, limited phase coherency, station clock input (SW 2.01)

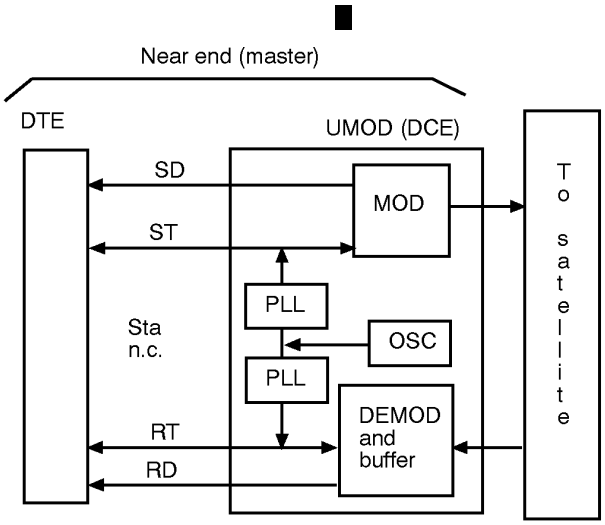

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Figure 3-50 Looped–timed, limited phase coherency, internal clock input (SW 2.01)

Looped–timed sys. phase coherent DTE

For software version 3.03 and higher. The examples shown in figures 3-51, 3-52, and 3-53 illustrate looped–timed systems with phase coherency, and assume the following:

- The DTE data rates are all the same
- The DTE requires a slaved phase relationship where no phase wander is allowed
- If TXDTE or station clock is used, input must be within ± 100 ppm
- For the *near* or *master* end, set Buffer ON and:
  - If TXDTE clock is used, set TCS to TXDTE (see figure 3-51)
  - If station clock is used, set TCS and RCS to Station (see figure 3-52)
  - If internal clock is used, set TCS and RCS to Internal (see figure 3-53)
- For the *far* or *slave* end, set Buffer OFF (RCS and TCS must be set to Recovered).

Note

These settings will also work if the DTE can accept phase wander.

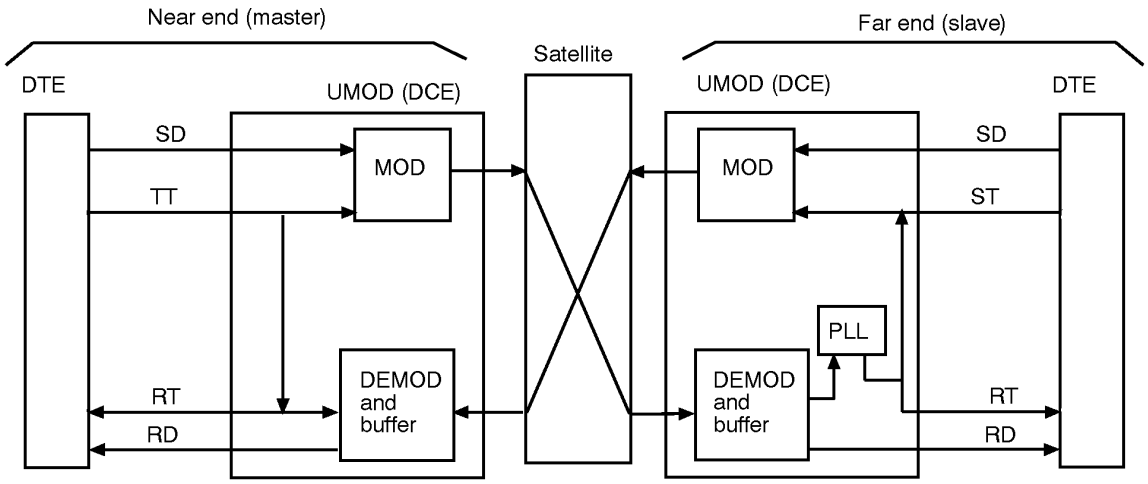

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Figure 3-51 Looped–timed, phase or limited phase coherent, using DTE clock (3.03)

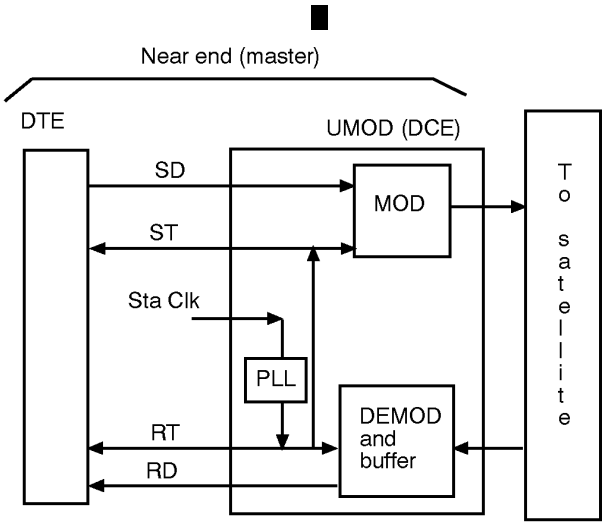

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Figure 3-52 Looped–timed, phase coherent using station clock input (SW 3.03)

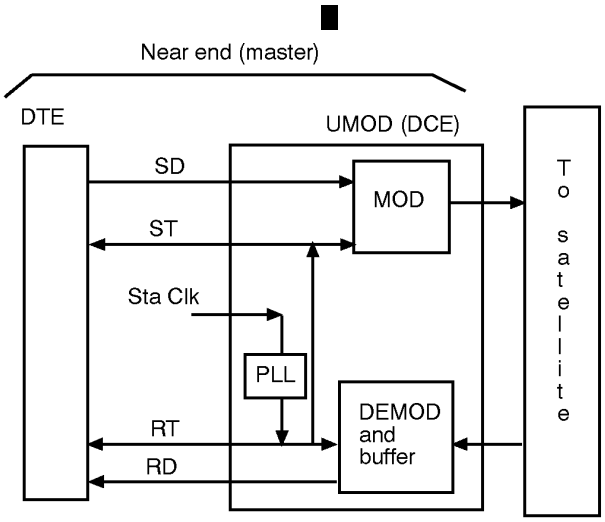

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Figure 3-53 Looped–timed, phase coherent, using internal clock input (SW 3.03)

Independent–timed systems

In an independently-timed system, the satellite link is operated with independent transmit and receive timing. The DTE device at each end of the link must be able to withstand propagation delays, along with transmit and receive clocks that may be far out of synchronization due to their independent operation. If an independent clock source configuration is selected, the satellite link is in effect, being operated as two independent one-way links. Data errors will not occur due to timing inconsistencies that might have otherwise have happened if they were sharing a common timing source.

If the link is operated with each UMOD supplying its own transmit and receive clock timing, be aware of the following:

- The two clock sources must be close enough in frequency that the number of bits slips that will occur are tolerable in the system over a given amount of time.
- There must be an elastic buffer in the receive path at each UMOD to negate propagation-related delay and phase differences between the receive timing source and the local clock, and then adjust the received data output to the DTE device.

This section describes independent–timed plesiochronous systems with phase coherent and limited phase coherent DTE for different software versions. Software versions are grouped as 2.01 and lower, and 3.03 and higher.

Independent–timed, phase coherent DTE

For software version 2.01 and lower. For an independent–timed plesiochronous system, you may use the modem's internal clock or an external station clock.

The examples shown in figures 3-54 and 3-55 assume the following:

- The DTE data rates are all the same
- The DTE requires a slaved phase relationship where no phase wander is allowed
- If the station clock is used, input must be well within ± 100 ppm, typically 10 or 1 ppm

Note

With software version 2.01 and lower, the DTE's internal clock cannot be used as a receive clock source.

- Set Buffer ON at both ends and:
  - If the modem's internal clock is used, TCS must be set to TXDTE, and RCS must be set to Station. Do not apply a signal to the station clock input (see figure 3-54)

- If the station clock is used, TCS must be set to TXDTE, and RCS must be set to Station (see figure 3-55)

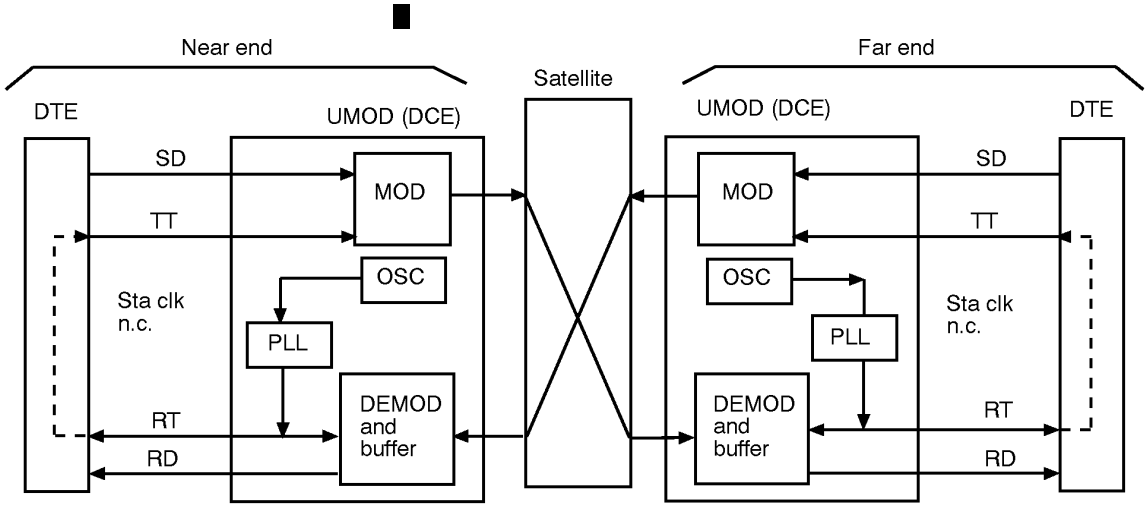

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Figure 3-54 Independent–timed, phase coherency w/o external clock (SW 2.01)

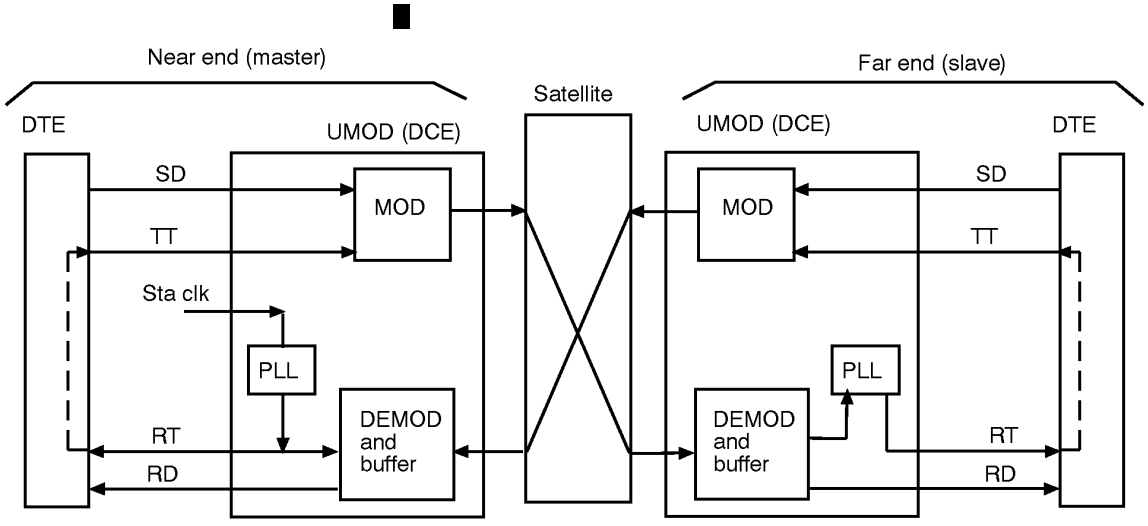

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Figure 3-55 Independent–timed, phase coherency with external clock (SW 2.01)

Independent–timed, limited phase coh. DTE

For software version 2.01 and lower. The examples shown in figures 3-56, 3-57, and 3-58 assume the following:

- The DTE data rates are all the same
- The DTE phase wander up to ±3 clock cycles of the lower frequency clock
- If the DTE's internal clock or station clock is used, input must be within ±100 ppm, typically 10 or 1 ppm
- Set Buffer ON at both ends and:
  - If the DTE's clock is used, set TCS and RCS to TXDTE. (see figure 3-56)
  - If the station clock is used, set TCS and RCS to Station (see figure 3-57)
  - For internal clock, set TCS to Internal, and RCS to Station (see figure 3-58)

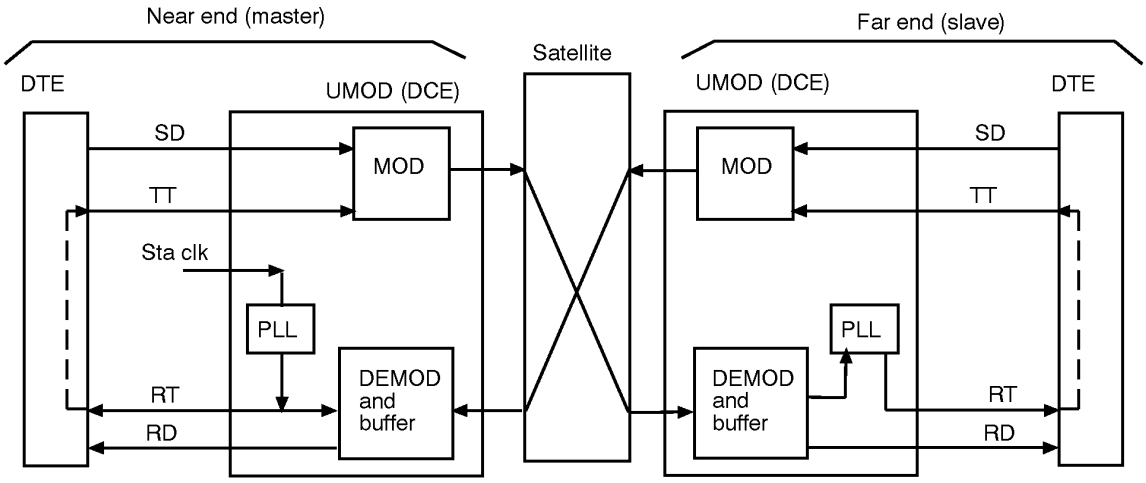

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Figure 3-56 Looped–timed,limited phase using DTE clock (SW 2.01)

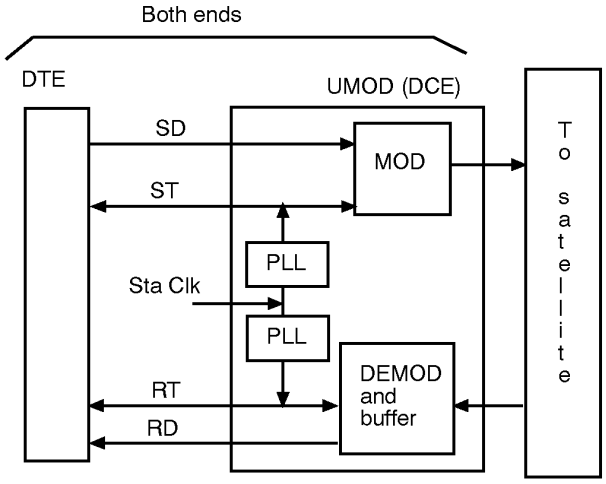

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Figure 3-57 Looped–timed,limited phase using station clock (SW 2.01)

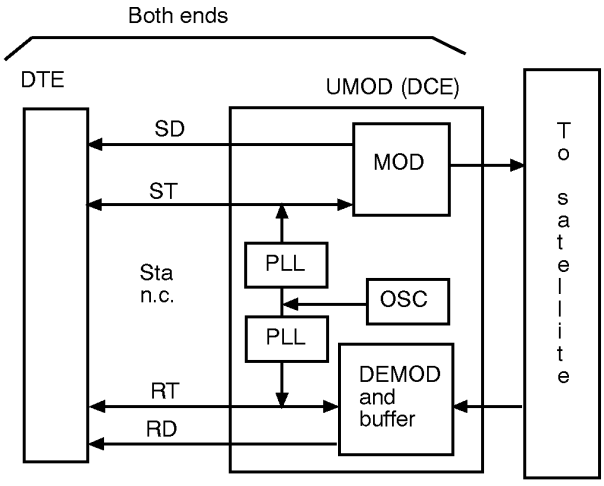

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Figure 3-58 Looped–timed, phase or limited phase using internal clock (SW 2.01)

Independent–timed, phase coherent DTE

For software version 3.03 and higher. For an independent–timed plesiochronous system, you may use the modem's internal clock or an external station clock.

The examples shown in figures 3-59, 3-60, and 3-61, assume the following:

- The DTE data rates are all the same
- The DTE requires a slaved phase relationship where no phase wander is allowed
- If station clock or TXDTE is used, input must be within ±100 ppm, typically 10 or 1 ppm
- Set Buffer ON at both ends and:
  - If DTE's clock is used, set TCS and RCS to TXDTE (see figure 3-59)
  - If station clock is used, set TCS and RCS to Station (see figure 3-60)
  - If UMOD's internal clock is used, set TCS and RCS to Internal (see figure 3-61)

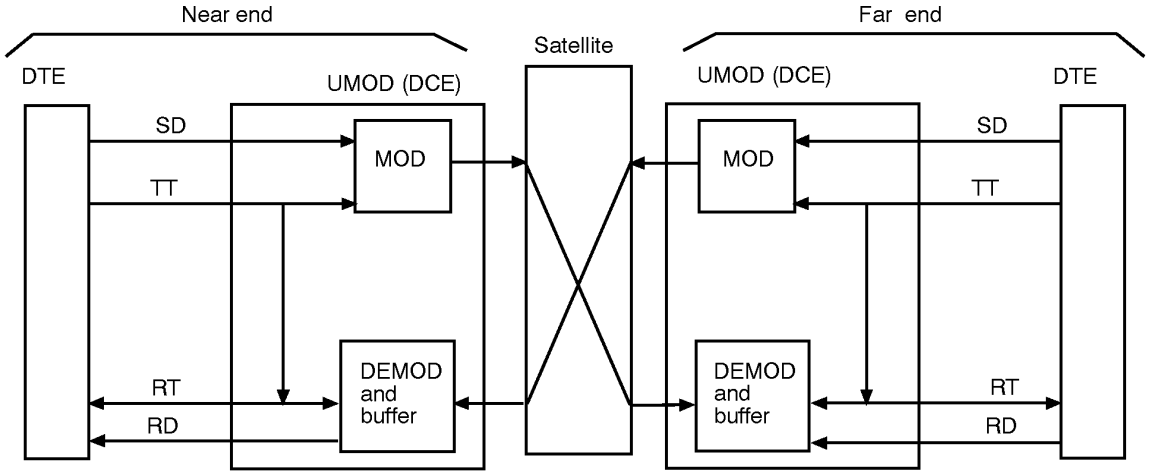

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Figure 3-59 Independent–timed, phase coherent using DTE clock (SW 3.03)

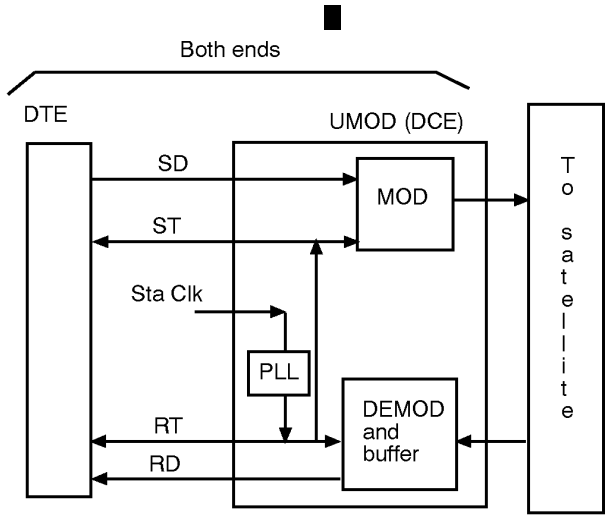

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Figure 3-60 Independent–timed, phase or limited phase, station clock (SW 3.03)

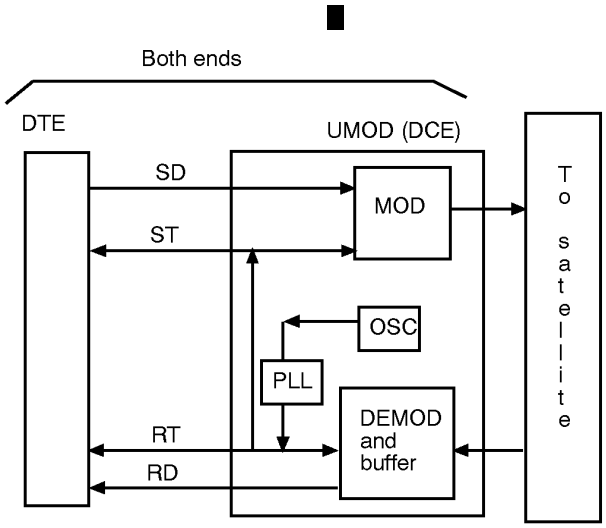

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Figure 3-61 Independent–timed, phase or limited phase, internal clock (SW 3.03)

Independent–timed, limited phase coh. DTE

For software version 3.03 and higher. The examples shown in figures 3-62, 3-63, and 3-64 assume the following:

- The DTE data rates are not the same
- The DTE will allow phase slips (wander) up to ±3 clock cycles of the slower clock
- If DTE's internal clock or or station clock is used, input must be within ±100 ppm, typically 10 or 1 ppm
- Set Buffer ON at both ends and:
  - If DTE's clock is used, set TCS and RCS to TXDTE (see figure 3-62)
  - If station clock is used, set TCS and RCS to Station (see figure 3-63)
  - For internal clock, set TCS and RCS to Internal (see figure 3-64)

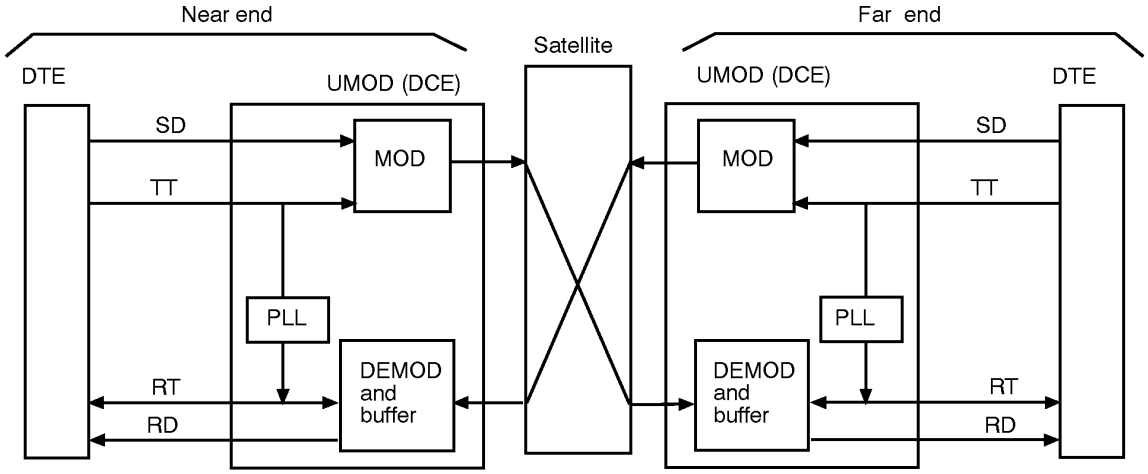

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Figure 3-62 Independent–timed, limited phase coherent using DTE clock (SW 3.03)

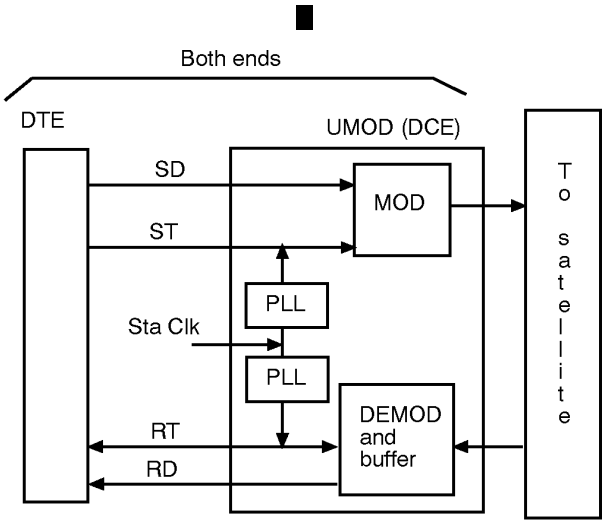

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Figure 3-63 Independent–timed, limited phase using station clock (SW 3.03)

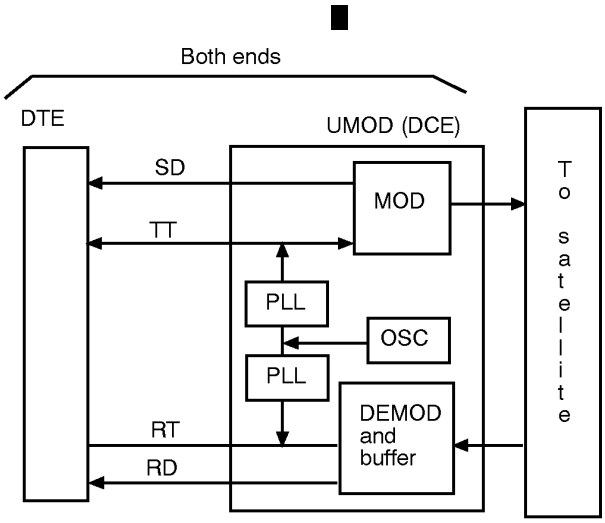

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Figure 3-64 Independent–timed, phase or limited phase, internal clock (SW 3.03)

Independent–timed non–plesiochronous

For these systems, virtually all clocking options apply because clock phase and frequency are independent on both links.

At each end, the transmit clock source (TCS) selections are: internal (INT), TXDTE (external TT), external station clock input (STA), and recovered from Demod (REC).

The RCS selections are: REC, TXDTE, and STA. For the software release 3.03 and above, there is a fourth mode, INT.

Chapter 4

Operational states

The UMOD operational states are:

- Initialization
- System diagnostics
- Signal acquisition
- Tracking
- Fade
- Idle

The following sections describe the operational states.

4.1 Initialization

At startup (or after a reset), the modem initializes—prepares for operation—the following UMOD hardware components:

- Terminal interface (M&C port)
- Front panel interface and LEDs
- Multidrop link (CIM ports P2 and P3)
- Microprocessor memory
- Modulator
- Encoder
- Demodulator
- Decoder
- Frequency synthesizers
- Terrestrial data interface daughtercard (DIM or GIM)
- Optional IFU
- Clock timing generators
- Terrestrial data interface

During initialization, the control processor (CP) scans the 0FFF:0 memory location in the 128–Kbyte TES boot EPROM firmware (see figure 4-1) to determine which operating mode will be used: UMOD operating mode or TES channel unit operating mode. The UMOD will always select UMOD operating mode (TES channel unit mode is used for another HNS product).

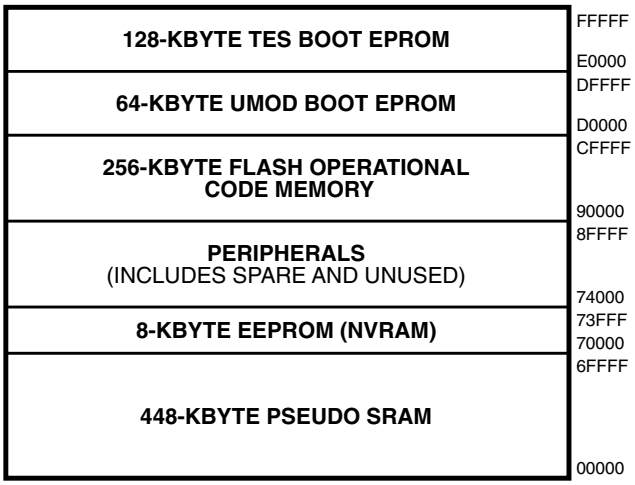

Figure 4-1 UMOD control processor memory map

Once UMOD operating mode has been selected, the CP activates the 64–Kbyte UMOD boot EPROM to begin the low–level hardware diagnostics tests. These tests verify that critical UMOD components such as memory and the microprocessor are functioning properly, and that the applications software loaded into the 256–Kbyte flash operational code memory has not become corrupt. Following successful completion of the diagnostics, the EPROM activates the applications software.

The applications software performs the following functions:

- System diagnostics
- Activating the front panel and M&C port drivers
- Configuring and controlling the modem hardware, multidrop link, and overhead channel link
- Carrier acquisition and tracking
- Providing IDR/IBS/SMS support
- Redundancy control
- Alarm monitoring and reporting

4.2

System diagnostics

The UMOD performs full–function diagnostics tests after initialization. These tests include:

- Performing an IF loopback test. In this test, the internal bit error rate (BER) tester loops data through the UMOD transmit and receive circuitry, including the terrestrial data interface daughtercard (either a DIM or GIM), and the optional internal framing unit (IFU). Once the BER tester verifies that the data it receives is error–free, the UMOD is operational.
- Verifying that there are no alarms
- Verifying the transmit power setting and testing the power detector

At the end of diagnostics, if the UMOD has been configured to autostart, it will begin the signal acquisition process. If autostart has been disabled, the UMOD will transition to the idle state.

4.3

Signal acquisition

In software, the acquisition process is comprised of three processing states: acquisition, track and fade. In the acquisition state, the modem sweeps to find a receive signal. Once the modem has found a valid receive signal, the modem considers itself to be in track mode and stops sweeping. When the modem is tracking a signal and loses lock, it considers itself to be in a fade. During a fade, the modem looks for the receive signal to reappear at the current frequency. If the signal does not reappear before the fade timeout expires, the modem restarts acquisition.

When the modem is successfully tracking a receive signal, the frequency offset information (see Figure 4-2) ftrack_offset is stored in EEPROM every 6 hours. The stored track frequency is then used when acquisition is initiated with an AUT ON or a redundancy switch.

Acquisition begins whenever the modem software is commanded to start sweeping for a receive signal. The sources of the acquisition start include user command, redundancy switch, AUT ON configuration setting, and reacquisition.

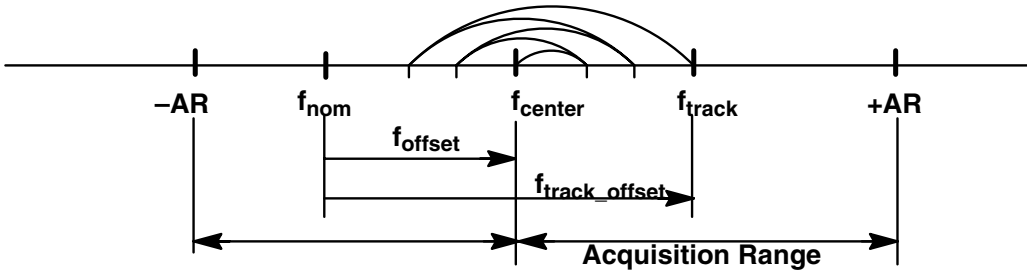

Figure 4-2 UMOD acquisition process

A user–initiated acquisition (with a GO or GO RX), the acquisition sweep starts at the center frequency, fcenter. The center frequency where acquisition sweep starts can be calculated by fcenter = fnom + foffset. The nominal frequency is entered with the RFQ command and the frequency offset is entered with the AO command.

Acquisition starts differently whenever it is initiated by a redundancy switch or by an AUT ON setting. Whenever these conditions cause acquisition to start, it can generally be assumed that some modem has previously been tracking a signal.

In Figure 4-2 the modem first looks for a valid receive signal at the frequency where it was previously located, ftrack. If a signal is not found there, the modem will then begin sweeping for a receive signal starting from the center frequency. The modem requires receipt of a minimum of 10000 symbols to determine whether a carrier is valid. This determines the time which the modem spends at each frequency during acquisition sweep.

4.4 Tracking

A transition from acquisition to tracking takes place only when the signal is locked for two consecutive samples. After the modem moves into track mode, the receive signal is monitored at one second intervals.

The track frequency offset and Eb/No are written into RAM at periodic intervals. An average of these values can be retrieved with the ST command. Also, every 6 hours, the track frequency offset is saved to EEPROM. The track frequency offset is also passed to the redundant modem during redundancy polling.

4.5 Fade

When the modem is tracking a signal and loses lock, it does not immediately begin acquisition sweep. Instead, the modem enters fade mode where it waits for the receive carrier to reappear at the current frequency. If the signal does not appear before the fade timeout expires, the modem will enter the acquisition stage and begin to sweep for a valid receive signal.The fade timeout value is user configurable with the ATF command.

4.6 Idle

While in the idle state, the UMOD is operational, but is not sending or receiving data. Modulator carrier power is set to off.

Chapter 5

Hardware installation

This chapter contains the following procedures for installing the hardware components of the 9100 Universal Modem 1-PAK chassis:

- Functional verification (page 5–3)—describes testing the UMOD to verify that it is operational before connecting it to the DTE device.

Note

Before installing the modem, the following tasks should have already been completed:

  - Assembling the antenna.
  - Installing the radio frequency (RF) unit onto the antenna.
  - Aligning the antenna toward the satellite.
  - Routing the interfacility link (IFL) cable from the antenna to the location where the modem will be installed.

- Rack mounting shelf installation (page 5–7)—describes installing the UMOD rack mounting shelf in a standard 19–inch rack.
- Cable installation (page 5–7)—describes installing the IFL and user equipment interface cables
- Installing the multidrop cables (page 5–9)—describes installing multidrop cables between as many as 30 Universal Modems.
- Setting the chassis ID code (page 5–11)—describes configuring UMOD switches to set the chassis identification (ID) code.
- Installing the redundancy cable (page 5–13)—If your UMOD is equipped for the redundancy option, refer to this procedure to install a redundancy cable between two UMOD chassis
- Completing the installation (page 5–14)—describes testing the UMOD to verify that it is operational.

5.1

Site preparation

Avoid installing the modem in a location where the ac power cord or input/output (I/O) cables could be accidentally disconnected. The location should be well ventilated. Do not set equipment on top of the modem or block its cooling vents. If the UMOD will be mounted in a 19–inch rack install the UMOD mounting shelf in the rack by performing the following procedure:

1. Place the rack mount shelf in position in the rack.
2. Secure the shelf in position with the four mounting screws provided.

5.2

Materials inspection

Inspect the shipping containers for external damage. Note any damage before opening the container. Report equipment damage to the shipping carrier immediately for claim purposes. Save all packing materials in case you need to return an item to the factory for servicing.

5.3

Tools and materials

You will need the following tools and materials for installing the Universal Modem:

- Flat blade screwdrivers, assorted sizes
- Phillips screwdriver
- Input/output (I/O) cables
- Shelf, rack mount 9100 UMOD HNS part # 1019180–0001

Functional verification

This section describes testing the UMOD to verify that it is operational before connecting it to the user's DTE device.

1. Remove the modem from its shipping container.
2. Place the modem at the designated location. Ensure that the O/| power switch is set to O (off). (See figure 5-1 for switch location.)

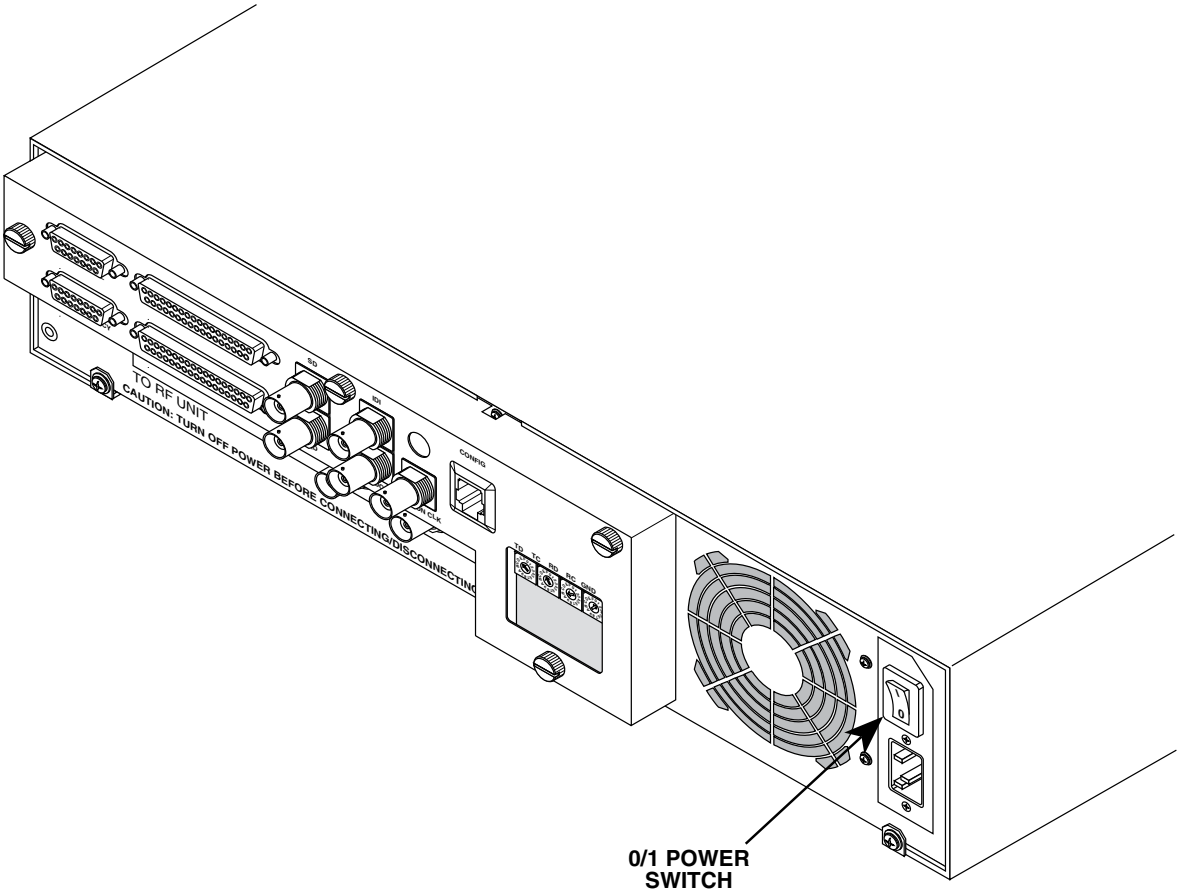

Figure 5-1 Universal Modem O/| power switch location

3. Route the IFL cable and all user equipment interface cables to the location where the modem will be installed.
4. Verify that the ac power cord included with your UMOD is compatible with local standards. If it is not, discard the cord and replace it with a compatible power cord.

Caution

The UMOD power supply automatically adjusts to accept an input voltage of from 100 to 240 Vac (47 to 63 Hz).

Verify that the proper voltage is present before plugging the ac cord into the receptacle. Failure to do so could result in equipment damage.

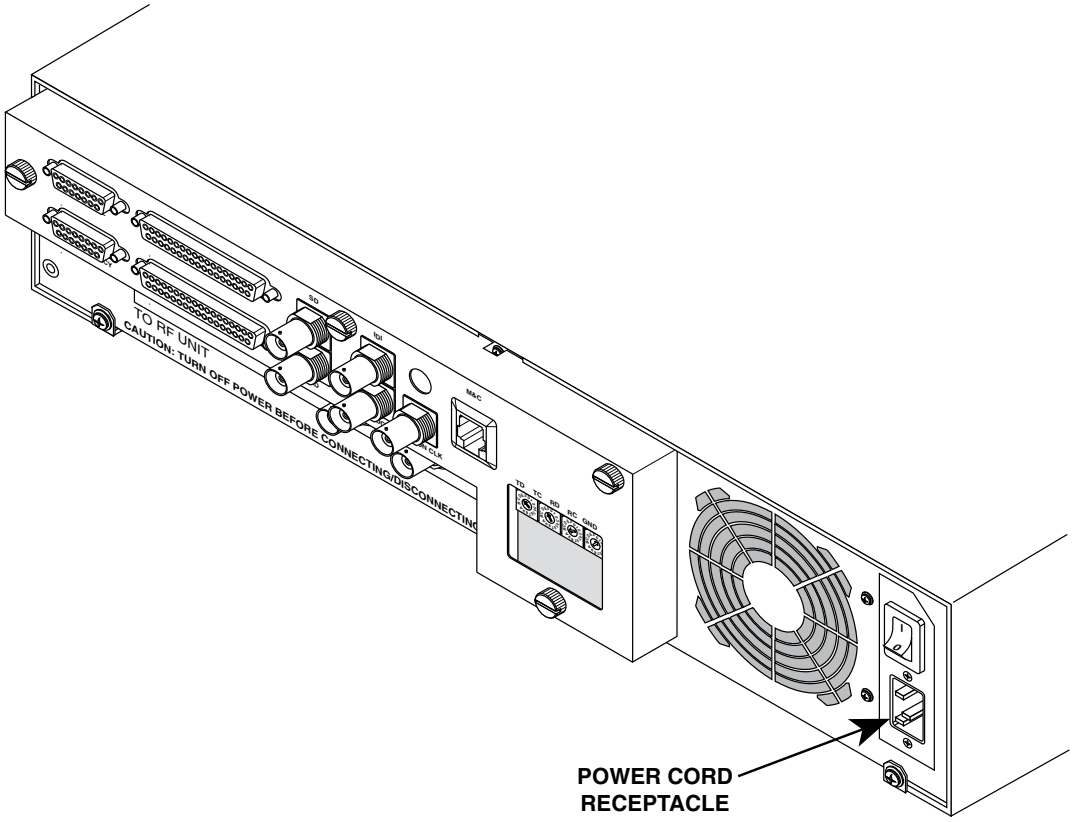

Figure 5-2 Power cord receptacle location

5. Connect the female end of the ac power cord into the receptacle (see figure 5-2). Connect the male end of the ac power cord to a power distribution strip or to a wall outlet.
6. Set the O/| power switch to | (activated).

Upon startup, the light-emitting diode (LED) on the UMOD front panel will begin cycling through a series of codes as the UMOD initializes its internal components and performs full-function diagnostics self-tests. (See figure 5-3 for LED location.)

If the tests are successful, you will see the sequence of displays on the LED readout as presented in table 5-1 . Each is a solid display, not flashing. The presence of a dot indicates that the UMOD board failed a test.

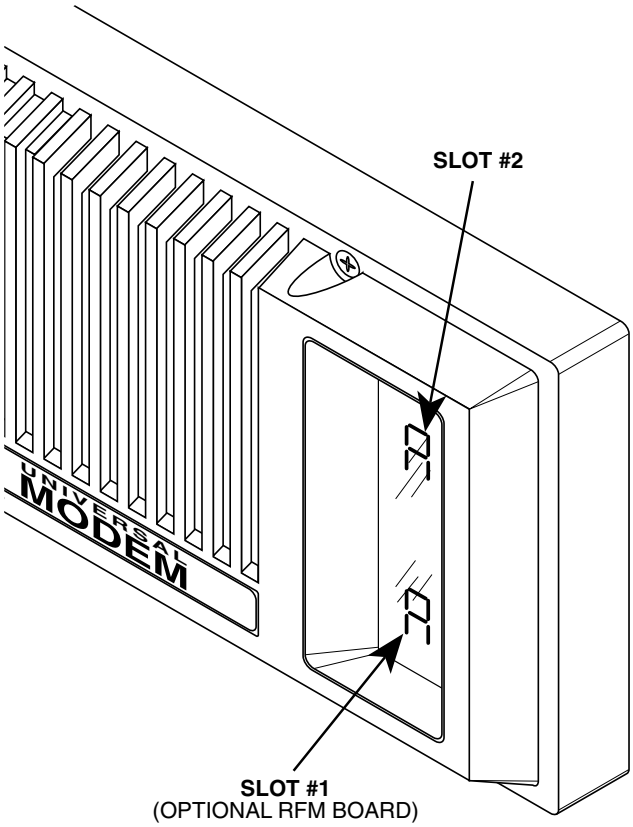

Figure 5-3 UMOD front panel LEDs

Table 5-1 UMOD self-test diagnostics

LED Display	Definition
0	Random access memory (RAM) test. This test writes a value to all RAM addresses, and verifies that the value can be read correctly.
1	Central processing unit (CPU) test. This test examines the microprocessor on the UMOD board
2	Internal timer test. This test examines the internal control processor timers.
3	DMA test. This test examines the direct memory access function.
4	QUART test. This test verifies that the quad-universal asynchronous receiver/transmitter (QUART) is functional.
5	SCC test. This test verifies that the serial communications controller (SCC) is functional.
6	SCC DMA test. This test verifies DMA access to the SCC.
7	Programmable interrupt controller (PIC) test. This test examines the internal PIC.
8	NVRAM test. This test computes the checksum for the non-volatile random-access memory (NVRAM) and compares it to the checksum stored in the last two bytes of NVRAM memory.
C	Flash code verification. This test verifies that the flash memory has not been corrupted by calculating the checksum and comparing the result to the stored value.
d	Full-function diagnostic. This test performs a full-function diagnostics test of the UMOD board. The internal bit error rate (BER) tester sends data through the transmit and receive circuitry, including the terrestrial data interface daughtercard (either a DIM or GIM), and the optional internal framing unit (IFU).
U	Idle mode. Once the UMOD has successfully completed the self-tests, it will go into idle mode.

Note

If a test fails, a decimal point will be added before the next test begins. For example, a failure in the DMA test would look like this: 3.

7. Verify after approximately 30 seconds, that a **U** is displayed on the UMOD light-emitting diode (LED). Also verify that the cooling fan is operating. If a test fails, refer to chapter 10, “Troubleshooting.”
8. Set the O/| power switch to O. Verify that the front panel LEDs are extinguished.

Refer to section 5.5, “Cable installation” on page 5–7 for procedures that describe installing the IFL and user equipment interface cables.

5.5

Cable installation

This section describes installing the IFL and user equipment interface cables.

1. This step describes installing the DTE device cables onto the CIM. Refer to table 5-2 to locate the desired connection type, then look for the checked (√) entries to determine which CIM connectors will be used.

Table 5-2 DTE-device-to-CIM interface cable configurations

	CIM Connectors				
Connection Type	TO DTE	G.703 BAL	ESC SIGNALS*	RD	SD
Balanced G.703		√	√		
Balanced G.703, single-bearer D&I		√	√		
Balanced G.703, twin-bearer D&I		√	√		
Balanced G.703, cascading D&I		√	√		
Unbalanced G.703			√	√	√
Unbalanced G.703, single-bearer D&I (preferred method)			√	√	√
Unbalanced G.703, single-bearer D&I (optional method)			√	√	√
Unbalanced G.703, cascading D&I			√	√	√
RS-449, RS-232, or V.35	√		√		

* Used with IDR, IBS, and SMS open-network framing.

2. Install the DTE interface cables onto the appropriate connectors on the CIM (see figure 5-4).
3. If your UMOD will be using an external clock source, connect the cable onto the STATION CLK port (see figure 5-4).

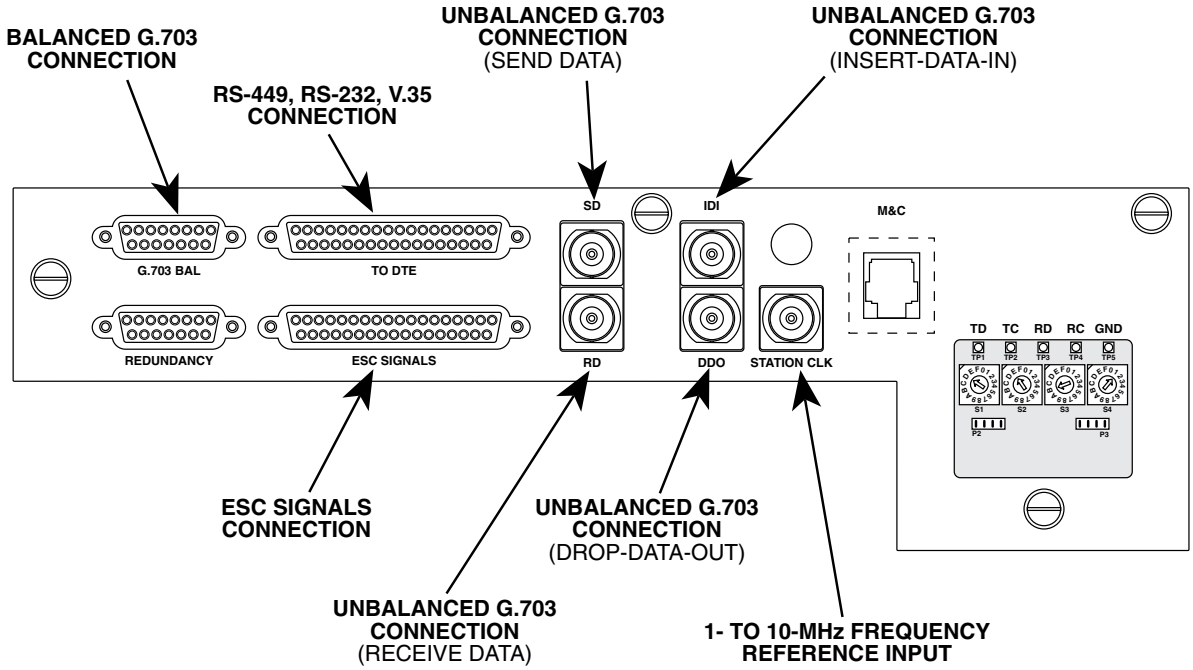

Figure 5-4 Customer interface module (CIM)

4. Install the IF IN cable onto the IF IN port on the IF panel (see figure 5-5 for location).
5. Install the IF OUT cable onto the IF OUT port on the IF panel (see figure 5-5).

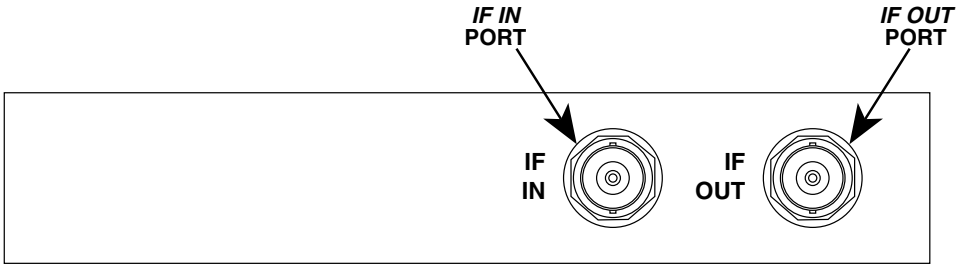

Figure 5-5 IF panel

Refer to section 5.6, “Installing the multidrop cables” on page 5–9.

Installing the multidrop cables

This section describes installing multidrop cables between as many as 30 Universal Modems. The multidrop cables link chassis together to form a monitor and control (M&C) network so that users can monitor UMOD status, and control many UMOD functions. The multidrop cables are connected to connectors P2 and P3 on the rear of the chassis. UMOD chassis #1 is wired to chassis #2; chassis #2 is wired to chassis #3; and so on until all chassis are connected (see figure 5-6).

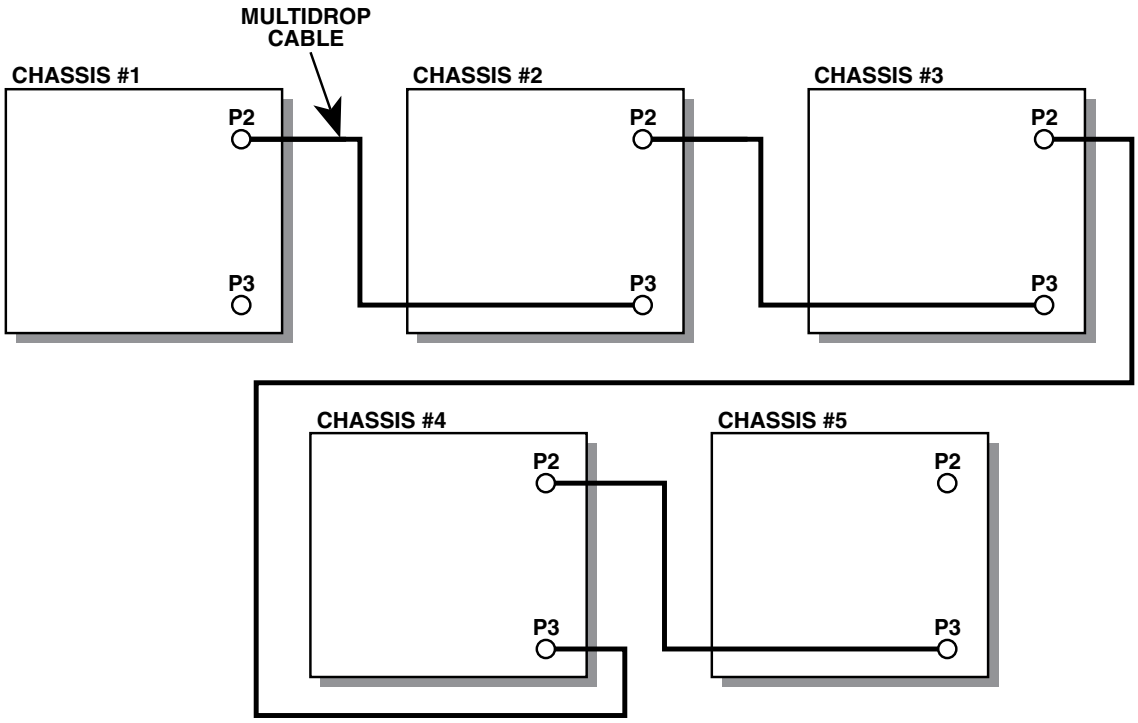

Figure 5-6 Example multidrop cable connection diagram for five UMOD chassis

1. Install a multidrop cable connector onto connector P2 on the first UMOD chassis (chassis #1). Connect the other end of the cable to connector P3 on chassis #2. See figure 5-7 for connector locations.

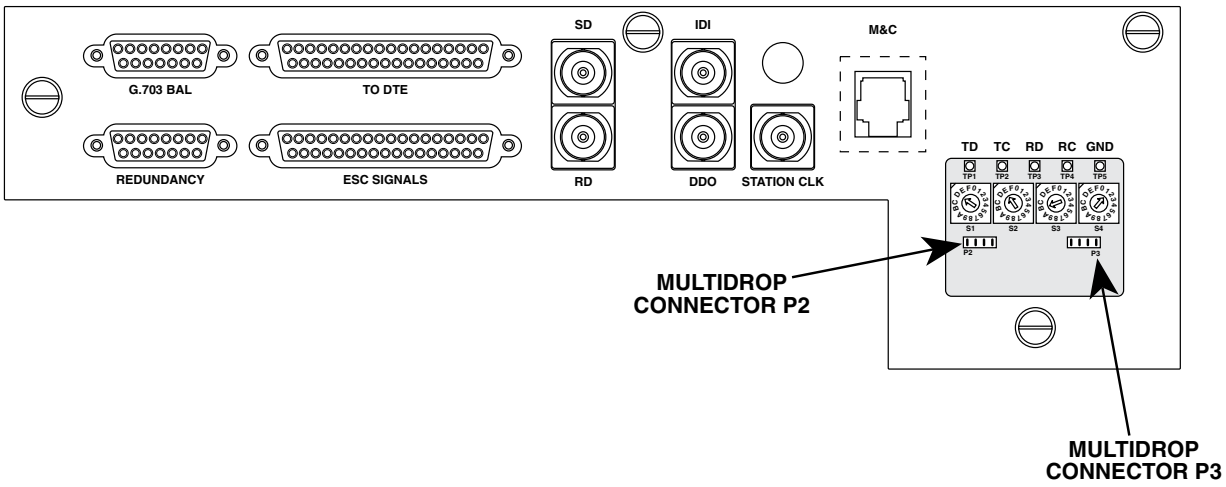

Figure 5-7 Multidrop connectors location

Perform the following procedure to install the multidrop cables.

2. Repeat step 1 to install multidrop cables between the remaining UMOD chassis as shown in figure 5-6.

Refer to section 5.7, “Setting the chassis ID code” on page 5–11.

Setting the chassis ID code

This section describes configuring switches S1 through S4 to set the chassis identification (ID) code (see figure 5-8 for locations).

Note

You need to obtain the four-digit hexadecimal chassis ID code before continuing. In this procedure, the example ID code will be *6 E B 1* (the same as that shown in figure 5-8).

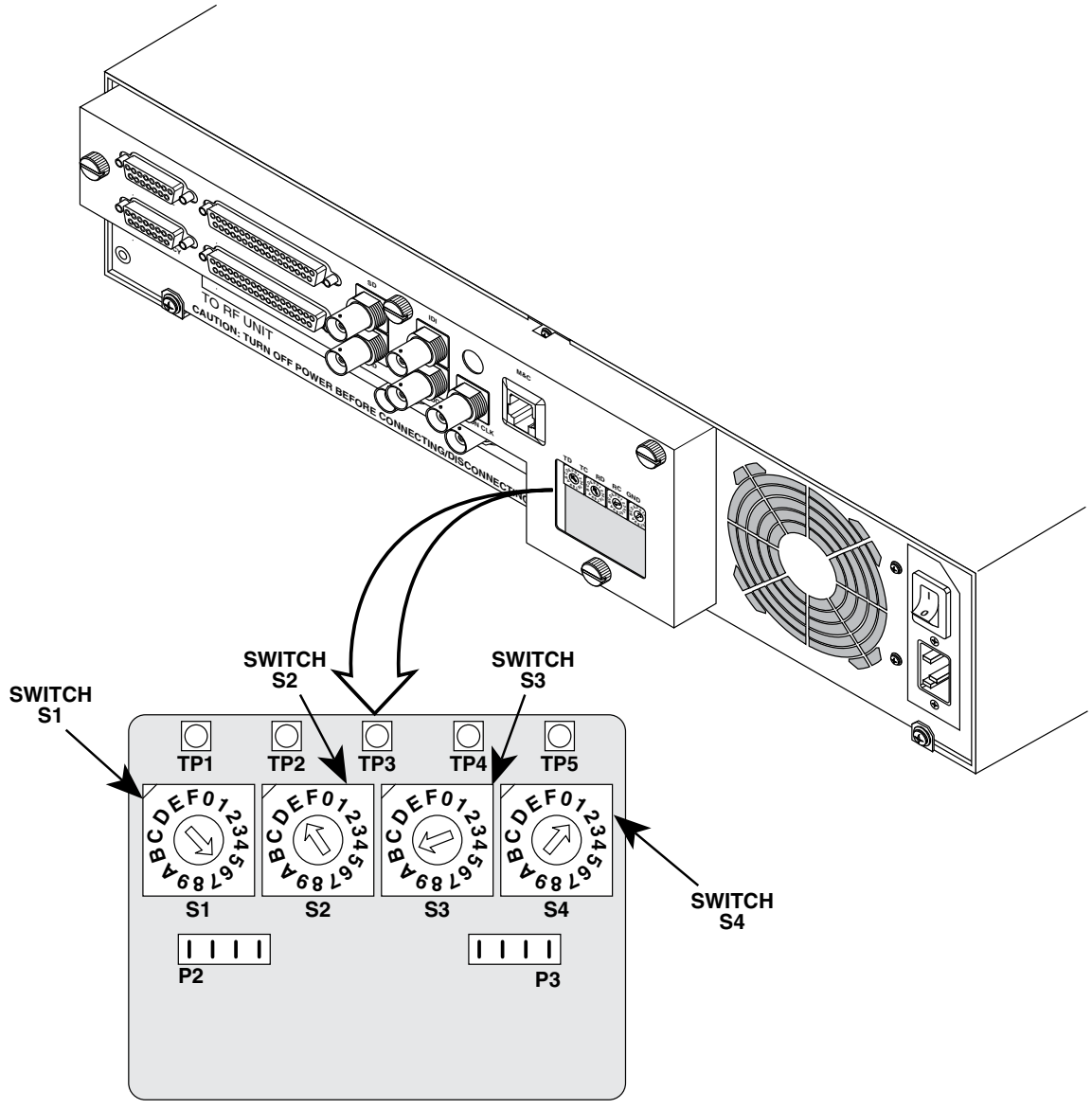

Figure 5-8 Chassis ID switches locations

Note

If you are using the redundancy option, both UMOD chassis must be set to the same ID code. (For example, if the primary UMOD ID code is 6EB1, the redundant UMOD would also be 6EB1.)

1. Using a 1/4-inch flat-blade screwdriver, set switch S1 to the same setting as the first (leftmost) hexadecimal digit in your chassis ID code. In the example this number would be *6*.

Note

The maximum UMOD chassis code setting is 7FFF, therefore switch S1 cannot be set to a higher setting than 7. Switches S2 thru S4 can each be set as high as F.

2. Set switch S2 to the same setting as the second digit in the code. In the example this number would be *E*.
3. Set switch S3 to the same setting as the third digit. In the example this number would be *B*.
4. Set switch S4 to the same setting as the fourth digit. In the example this number would be *1*.

If your UMOD will be connected to a redundant UMOD chassis, refer to section 5.8, “Installing the redundancy cable” on page 5–13. Otherwise, refer to section 5.9, “Completing the installation” on page 5–14.

Installing the redundancy cables

Perform the following procedure to install the redundancy cables between two single slot UMOD chassis.

1. Install the end of the redundancy cable connector labeled PRIMARY onto the REDUNDANCY connector on the primary UMOD chassis (see figure 5-9).

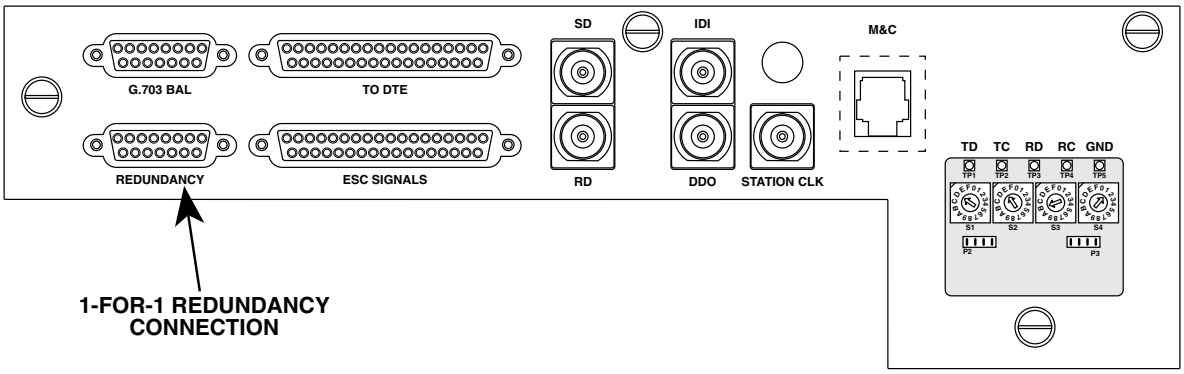

Figure 5-9 Redundancy connector location

2. Install the remaining end of the cable onto the redundant UMOD chassis.
3. If the customer equipment interface is RS–449, V.35 or RS–232 install the“Y” ends of the DTE–Y redundancy cable onto the TO DTE connector on the primary and redundant UMOD chassis.
4. Install the remaining end of the cable onto the customer equipment.
5. If the customer equipment interface requires G.703 signalling install the“Y” ends of the G.703 redundancy cable onto the G.703 BAL connector on the primary and redundant UMOD chassis.
6. Install the remaining end of the cable onto the customer equipment.
7. Install the”Y” ends of the ESC redundancy cable onto the ESC SIGNALS connector on the primary and redundant UMOD chassis.
8. Install the remaining end of the cable onto the customer equipment.

Refer to section 5.9, “Completing the installation” on page 5–14.

Completing the installation

This section describes testing the UMOD to verify that it is operational.

1. Set the O/| power switch to | (activated).

   Upon startup, the LED on the UMOD board will begin cycling through a series of codes as the UMOD initializes its internal components and performs full-function diagnostics self-tests.

Table 5-3 UMOD startup tests

LED Display	Definition
0	Random access memory (RAM) test. This test writes a value to all RAM addresses, and verifies that the value can be read correctly.
1	Central processing unit (CPU) test. This test examines the microprocessor on the UMOD board
2	Internal timer test. This test examines the internal control processor timers.
3	DMA test. This test examines the direct memory access function.
4	Q-UART test. This test verifies that the quad-universal asynchronous receiver/transmitter (Q-UART) is functional.
5	SCC test. This test verifies that the serial communications controller (SCC) is functional.
6	SCC DMA test. This test verifies DMA access to the SCC.
7	PIC test. This test examines the internal PIC.
8	NVRAM test. This test computes the checksum for the non-volatile random-access memory (NVRAM) and compares it to the checksum stored in the last two bytes of NVRAM memory.
C	Flash code verification. This test verifies that the flash memory has not been corrupted by calculating the checksum and comparing the result to the stored value.
d	Full-function diagnostic. This test performs a full-function diagnostics test of the UMOD board. The internal bit error rate (BER) tester sends data through the transmit and receive circuitry, including the terrestrial data interface daughtercard (either a DIM or GIM), and the optional internal framing unit (IFU).

If the tests are successful, you will see the sequence of displays on the card's LED as presented in table 5-3 . Each is a solid display, not flashing. The presence of a dot indicates that the UMOD board failed a test.

2. Depending on how your UMOD is configured, once the full-function diagnostics are complete one of the following LED codes will be displayed:
   - If the UMOD is configured for autostart operation, it will display an **A** to indicate that it is acquiring a carrier, then display an **L** to show that it has locked onto the carrier signal.
   - If autostart operation is disabled, the UMOD will display a **U** to indicate that it is in idle mode but ready to begin operation.
   - If redundancy is in use and the UMOD is configured as the redundant modem, it will display an **r** to indicate that it currently polling the primary modem's status.

Hardware installation is now complete, refer to chapter 6, "Configuring the UMOD for operation."